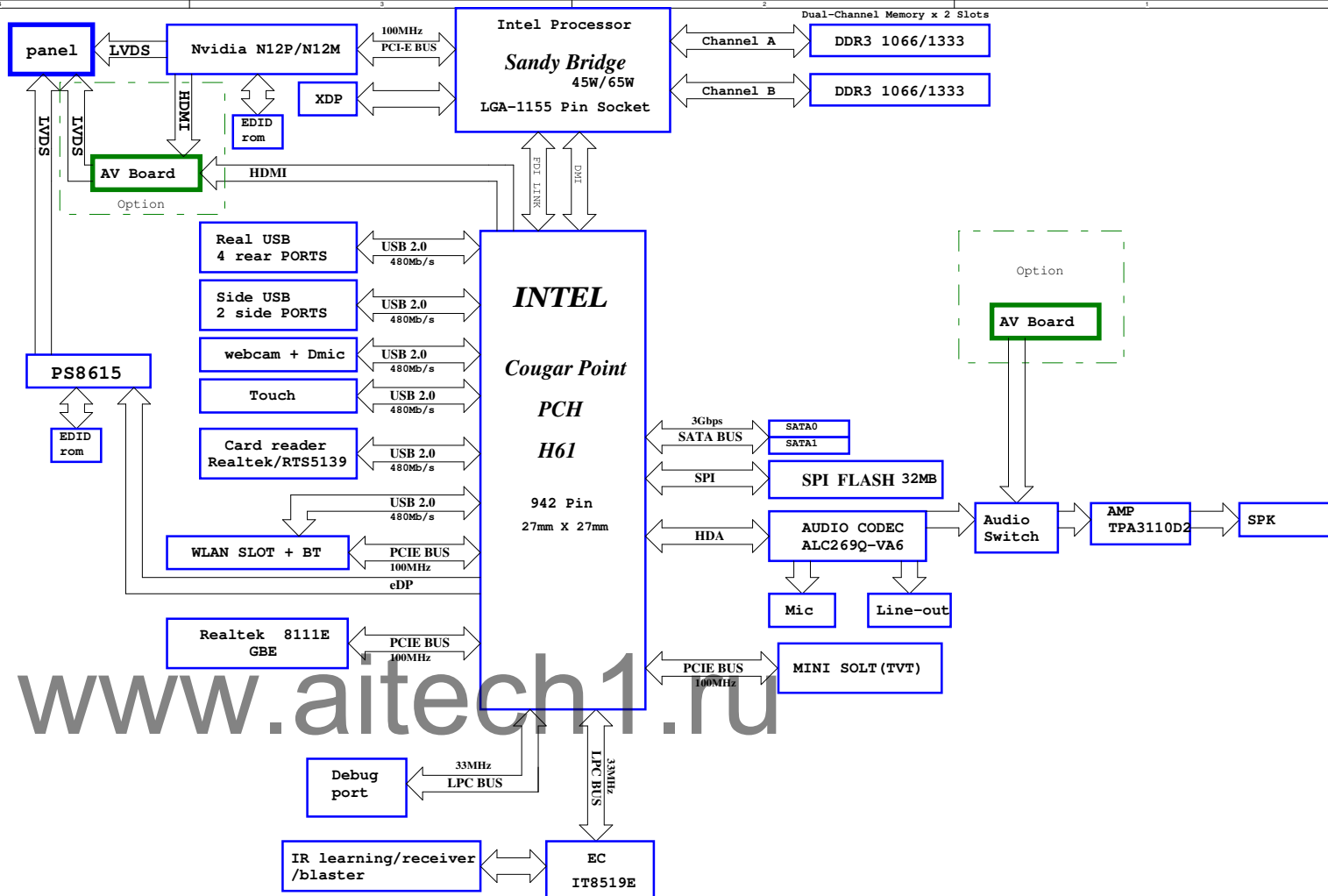


IPPSB-FA

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER FLOW
03	POWER SEQUENCE
04~09	CPU LGA1155 DDR3 A 1-6
10	DDR3 CHANNEL A G/F
11	DDR3 CHANNEL B G/F
12	DDR3 TERMINATION A&B
13	PLTRST CPU# & Smbus
14	Converter Controller
15~16	LVDS&AV CONN
17~25	INTEL_PCH 1-9
27~28	LAN
29~30	CODEC&CONN
31~32	AMP&SWITCH
33~35	USB&HUB&BT
36	HPD_DET
37~38	MINI_CARD (WL&TVT&DMC)
39	Misc. conn&Touch&Wcam&RTC
40	FAN
41	PWR_LED & Button*
42	IR_LEDS
43~44	EC 8519
45	SM BUS & SPI ROM
46	SCREW HOLE
47	UVF, OVP & +19VSB
48	LOAD_SWITCH
49	+3P3VSB&+5VSB
50	+1P5V_DUAL & +1P2V
51	Current Monitor
52	+12V & +1P8V
53	+1P05V_CPUIO&+0P925V_SA
54	POWER_PROTECT
55	+1P05V_CPUIO_CAP
56	+VTT_DDR
57	+V_AXG DRIVER
58	+VCORE CONTROLLER
59~61	+VCORE_CAP
62	+1P05V&+1P05V_PCH
63~64	CPU&PCH_XDP_DEBUG_CONNECTOR
65	VGA_CONN
66~67	GPU_DDR3
68	VGA-N12P_STRAPPING&EEPROM
69	MXM.VGA-N12P_Xtal/Thermal
70~71	GPU_HDMI (DMC&AV)
72	GPU_CTRL
73	GPU.VGA_N12P_PCI-E I/F
74	GPU_PCI-E_LVDS_VGA
75	MXM.GPU_Discharge
76	GPU_POWER&GND
77	MXM.NVDD
78	Card Reader RTS5139-GR
79	EDP_CH7511



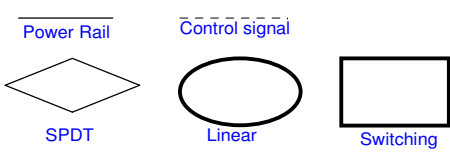
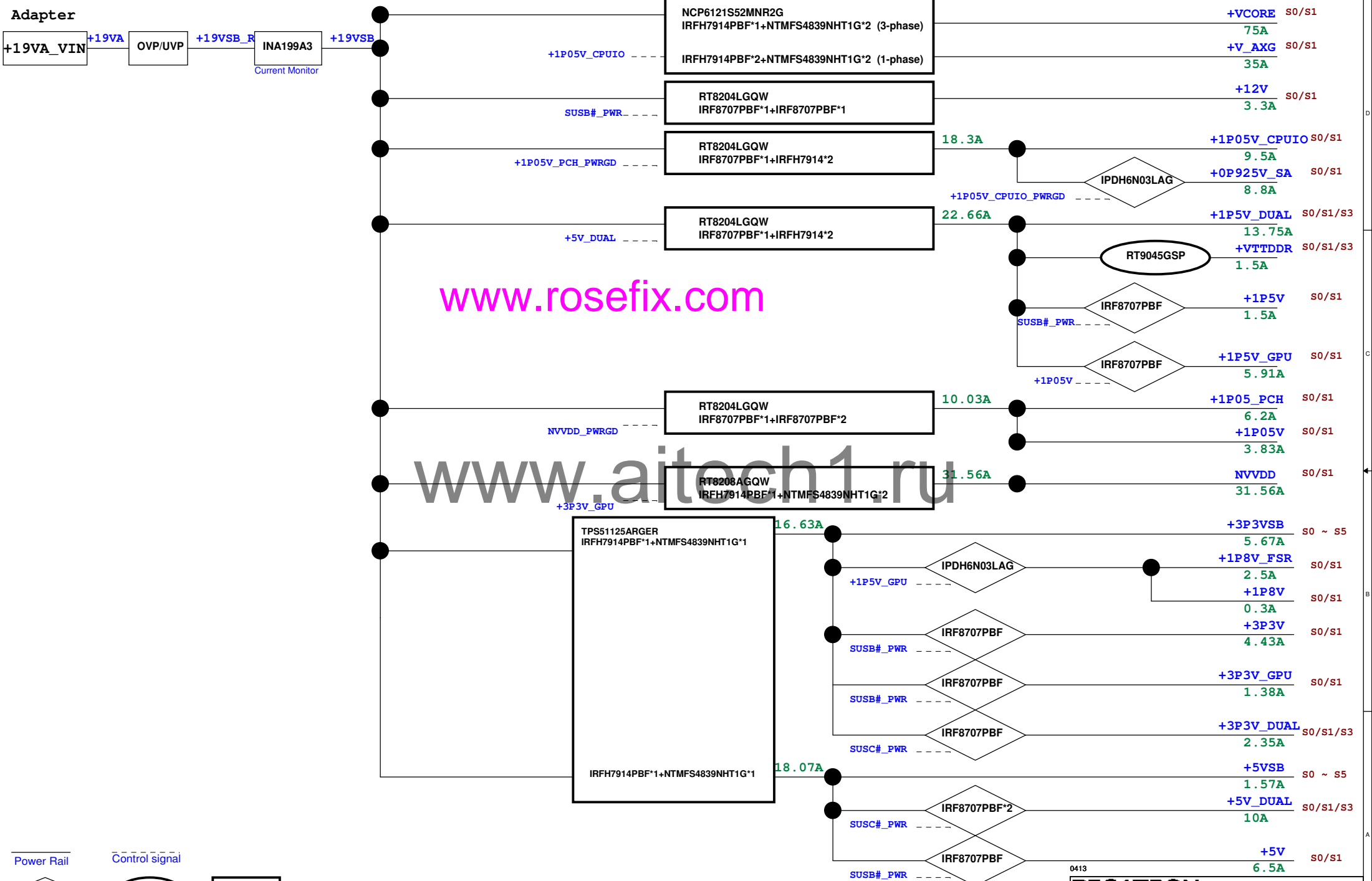
PEGATRON DT-MB RESTRICTED SECRET

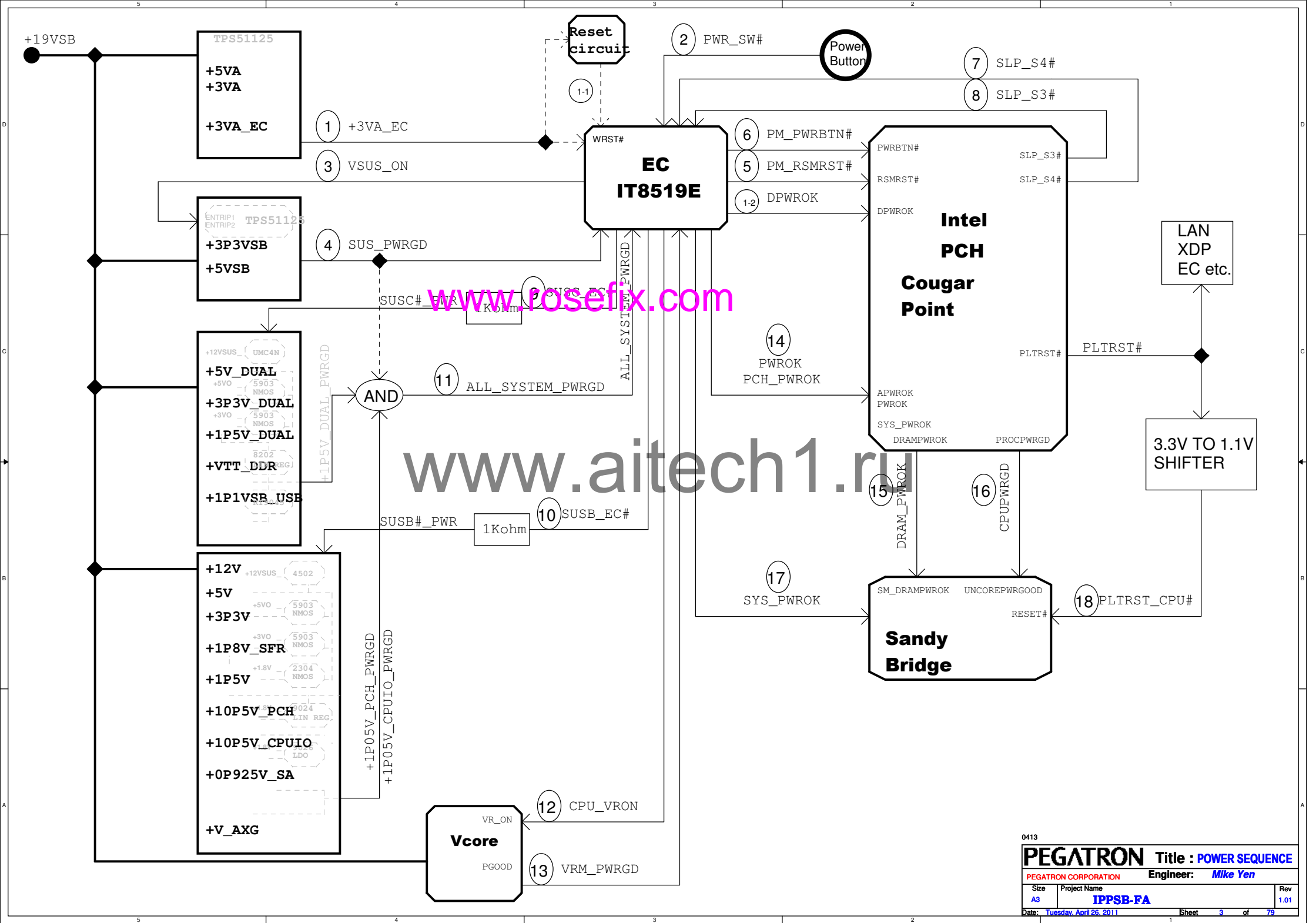
PEGATRON Title : BLOK DIAGRAM

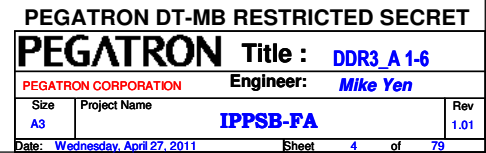
PEGATRON CORPORATION Engineer: Jerry Chung

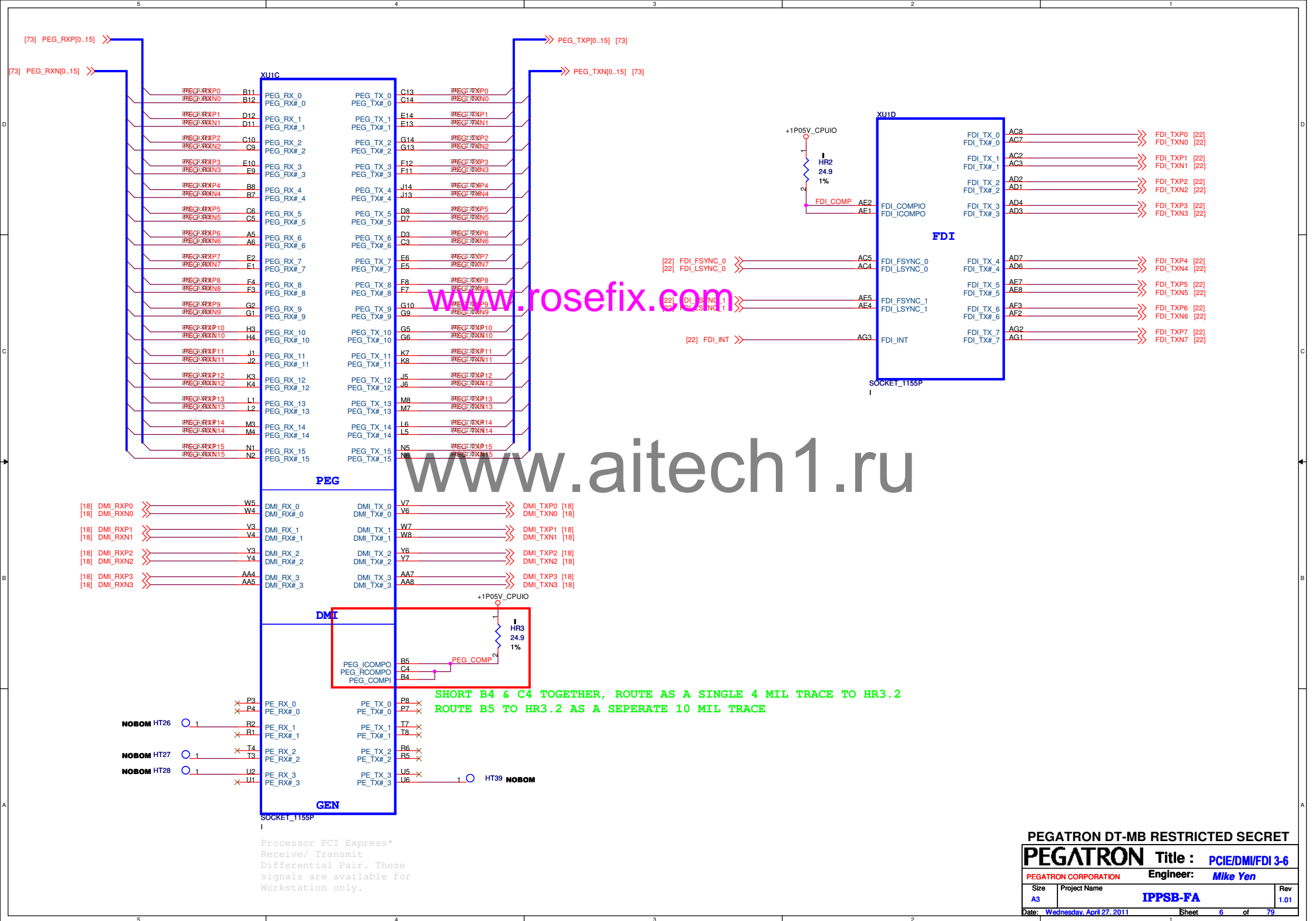
Size Project Name IPPSB-FA Rev 1.01

DATE: Tuesday, April 28, 2011 Sheet 1 of 79









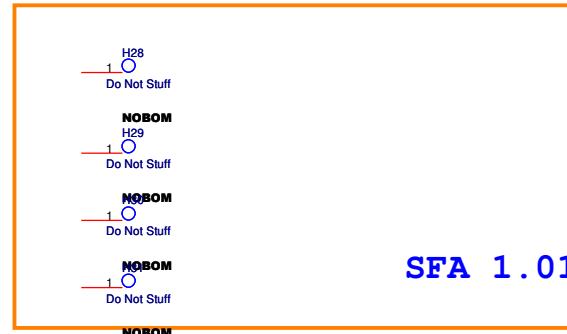
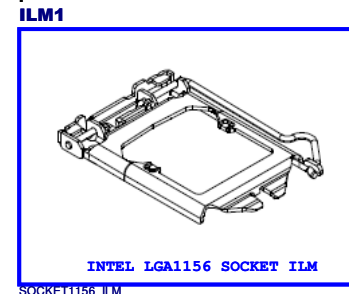
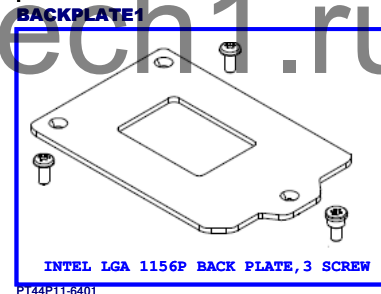
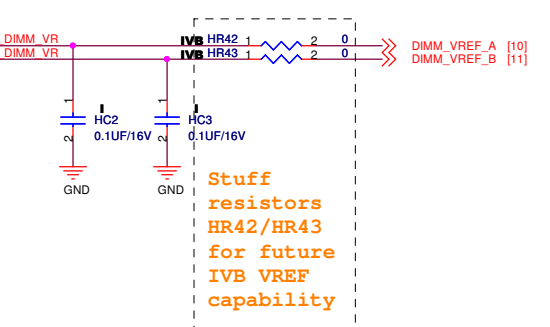
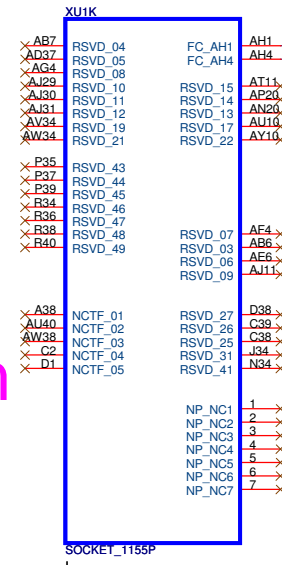
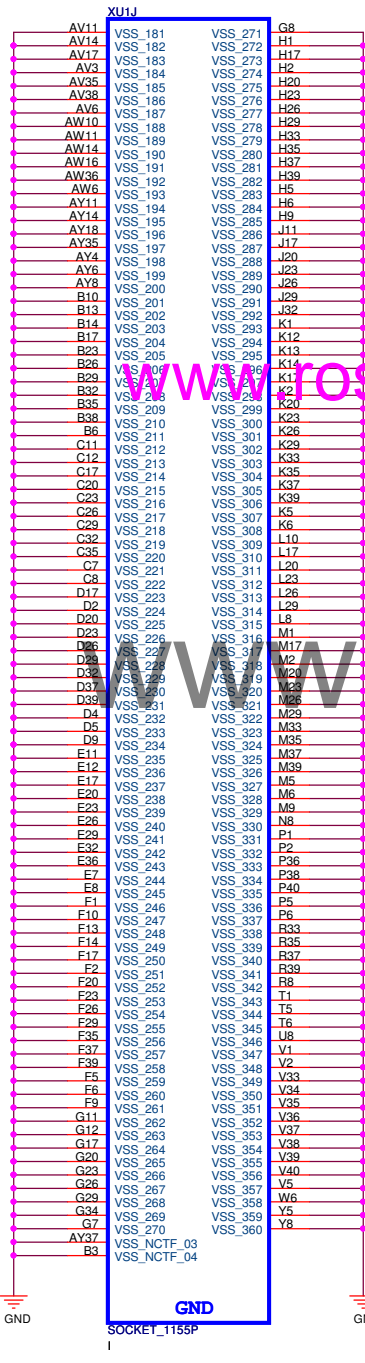
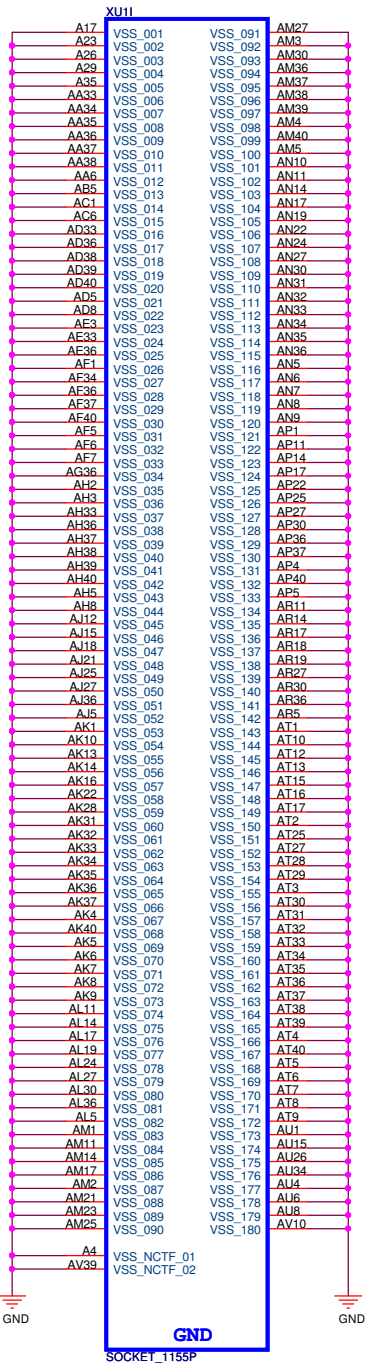
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **PCIE/DMI/FDI 3-6**

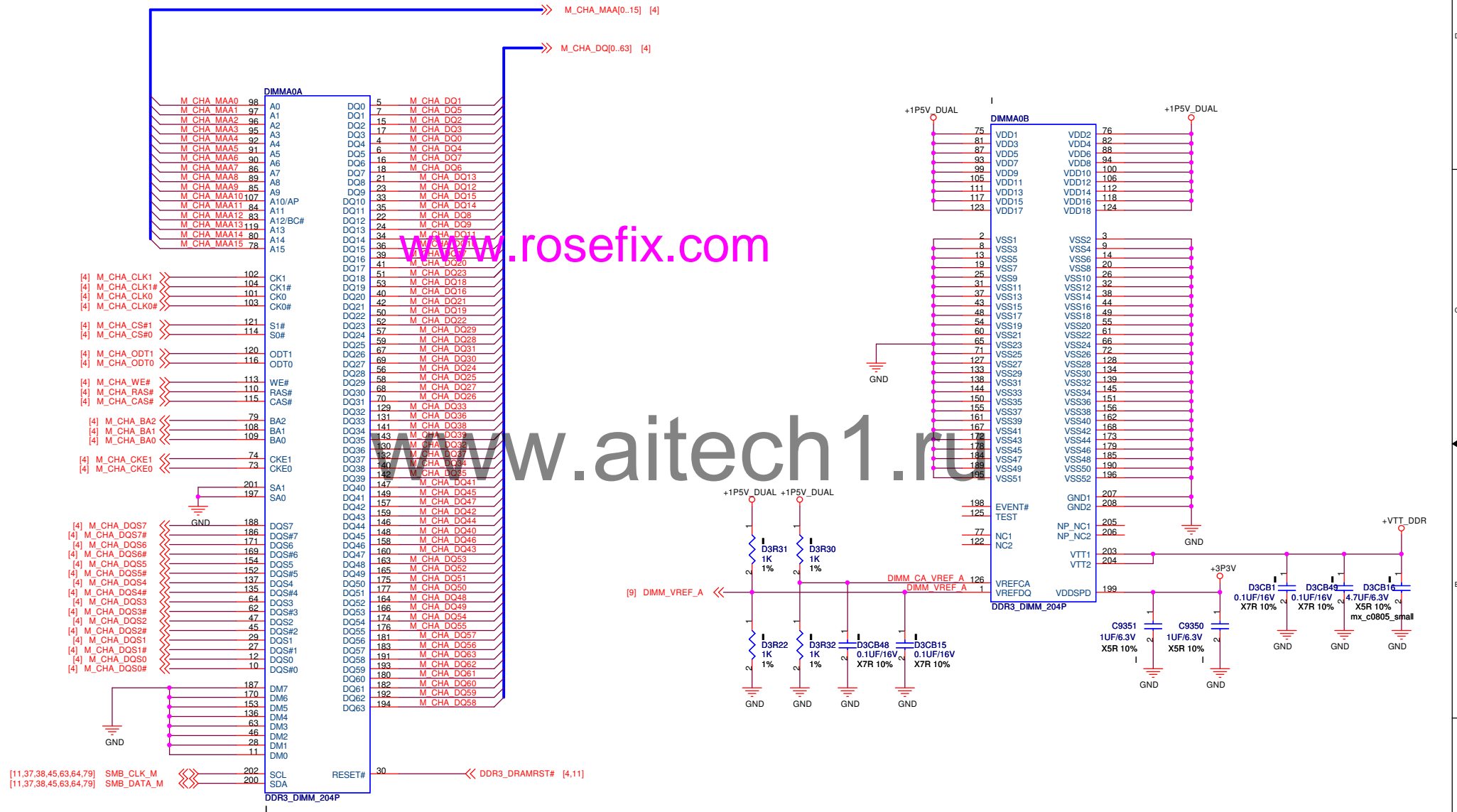
PEGATRON CORPORATION Engineer: **Mike Yen**

Size	Project Name	Rev
A3	IPPSB-FA	1.01

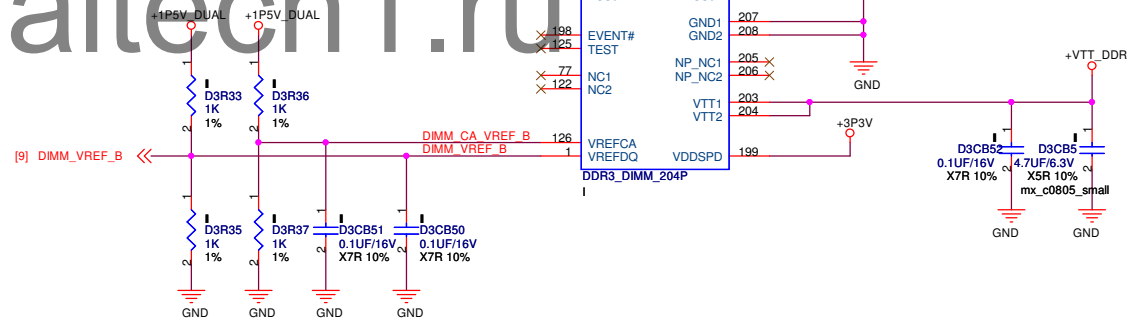
Date: **Wednesday, April 27, 2011** Sheet **6** of **79**

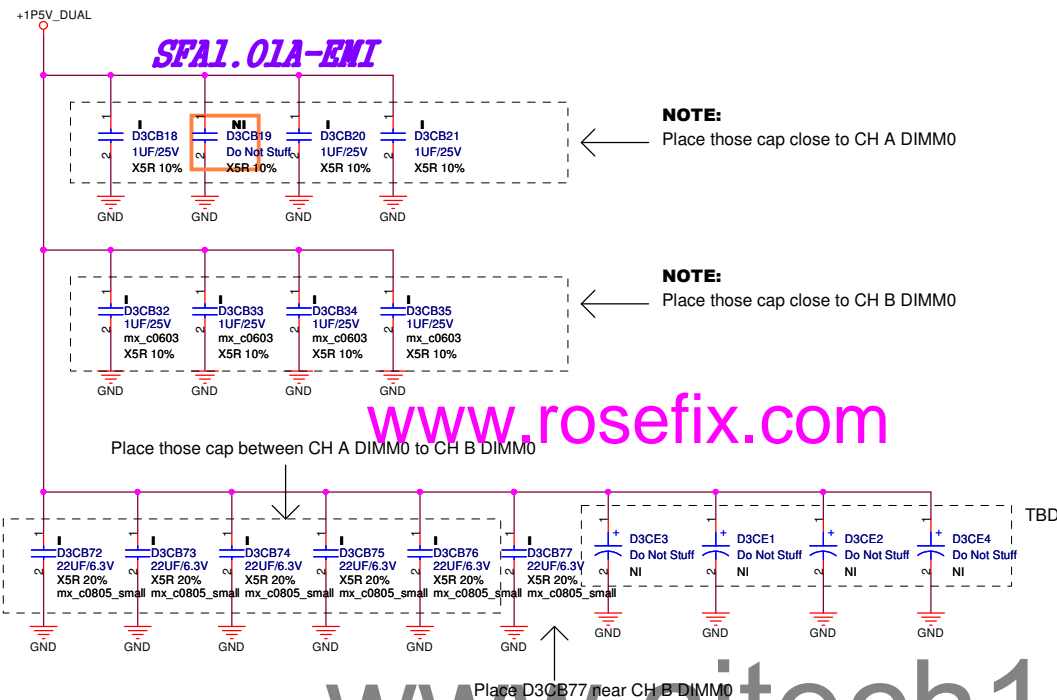


皆改爲5.2H



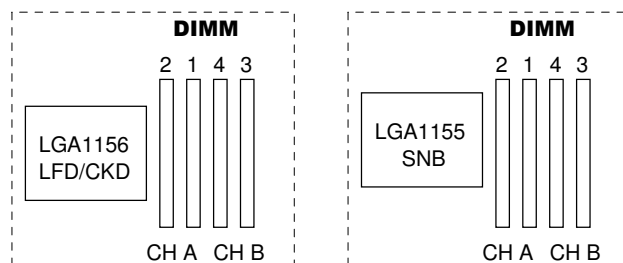
www.rosefix.com





NOTE:

DIMM Placement for different platform



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 TERMINATION A&B

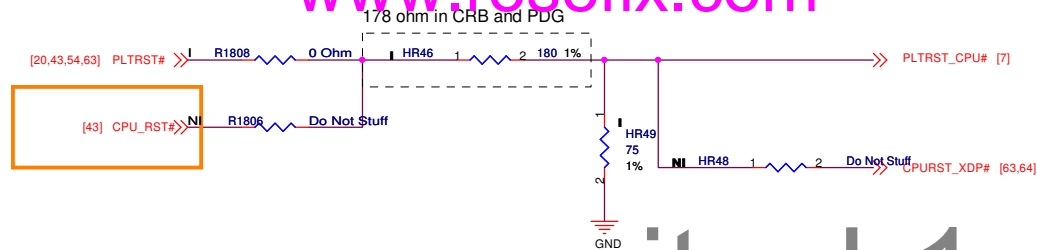
PEGATRON CORPORATION Engineer: Mike Yen

Size A3	Project Name IPPSB-FA	Rev 1.01
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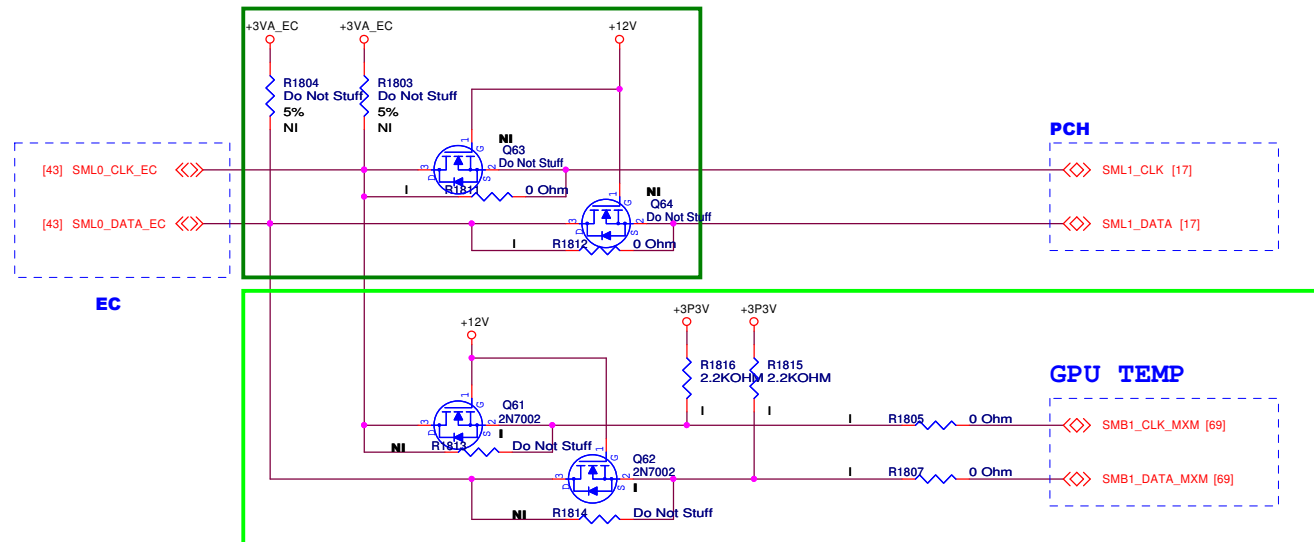
Date: Tuesday, April 26, 2011 Sheet 12 of 79

PLTRST_CPU#

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www.aitech1.ru



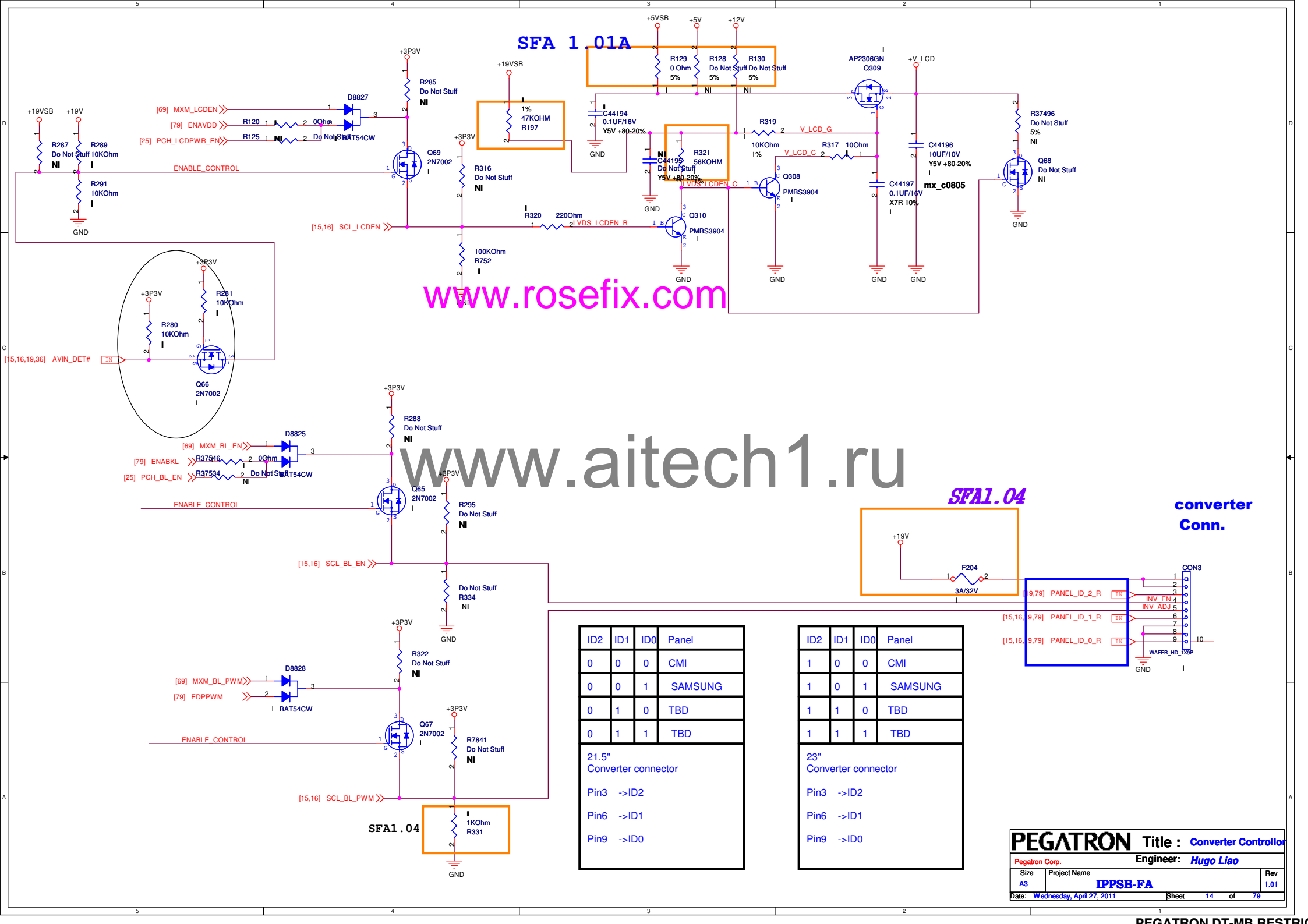
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PLTRST_CPU#&SMBus

PEGATRON CORPORATION Engineer: XXXX-XX

Size A3	Project Name IPPSB-FA	Rev 1.01
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Date: Wednesday, April 27, 2011 Sheet 13 of 79



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www.aitech1.ru

SFA1.04

converter
Conn.

ID2	ID1	ID0	Panel
0	0	0	CMI
0	0	1	SAMSUNG
0	1	0	TBD
0	1	1	TBD

21.5"
Converter connector

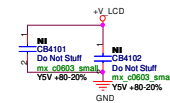
Pin3 ->ID2
Pin6 ->ID1
Pin9 ->ID0

ID2	ID1	ID0	Panel
1	0	0	CMI
1	0	1	SAMSUNG
1	1	0	TBD
1	1	1	TBD

23"
Converter connector

Pin3 ->ID2
Pin6 ->ID1
Pin9 ->ID0

LCD CONN NB & GPU colay



www.aitech1.ru

已修改 未完成



LVDS CONN (GPU)



www.aitech1.ru

已修改 未完成



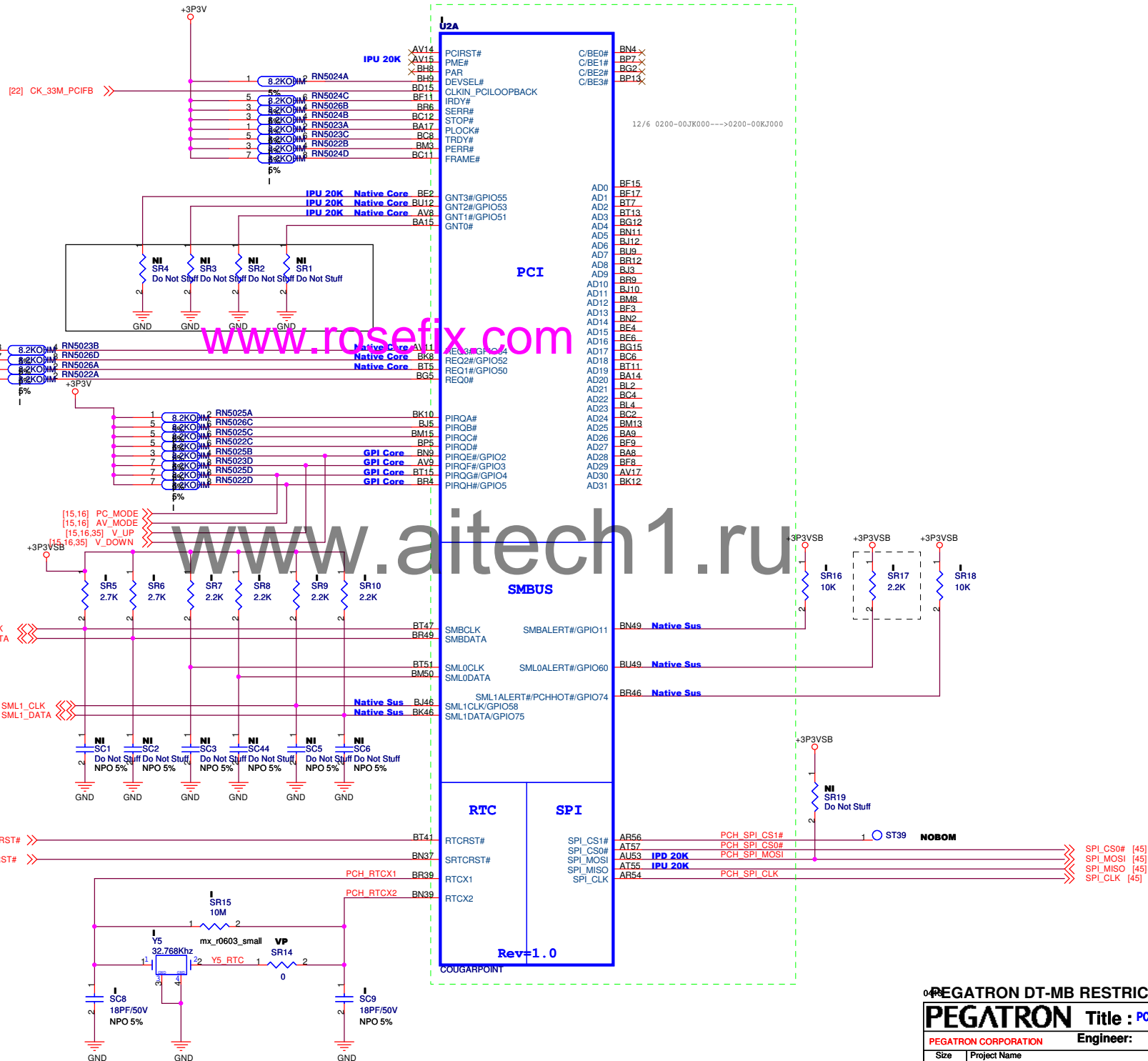
EMI修改

PEGATRON		Title : LVDS CON	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name		R
A2	IPPSB-FA		1/

NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

I2C/en(dis)able/S3
for accelerometer



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCI/SM/SPI/RTC 1-9

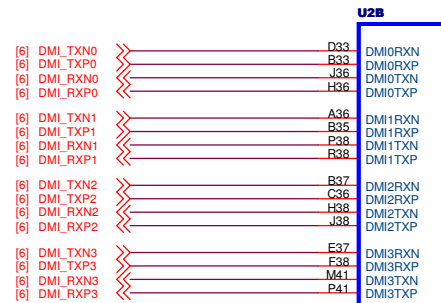
PEGATRON CORPORATION Engineer: Mike Yen

Size	Project Name	Rev
A3	IPPSB-FA	1.01

Date: Wednesday, April 27, 2011 Sheet 17 of 79

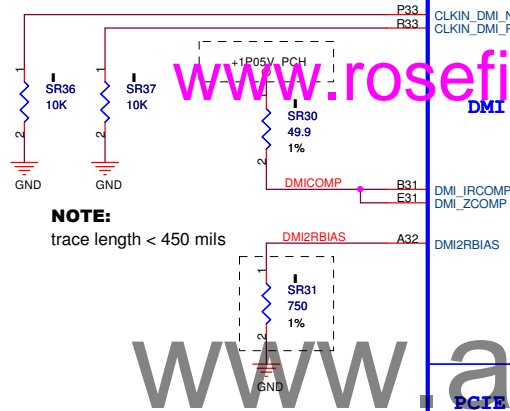
NOTE:

Used for for DMI, PCIe(PCIe 2.0 jitter spec compliant).

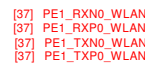


NOTE:

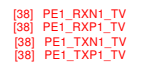
trace length < 450 mils



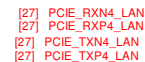
WLAN



TVT



LAN



for H61,
PCIe ports 7 and 8 are disabled.

NOBOM	ST16	0	1	TP	PCH	RN7	J12
NOBOM	ST14	0	1	TP	PCH	RP7	H12
NOBOM	ST13	0	1	TP	PCH	TN7	E15
NOBOM	ST15	0	1	TP	PCH	TP7	F13
NOBOM	ST9	0	1	TP	PCH	RN8	H10
NOBOM	ST10	0	1	TP	PCH	RP8	J10
NOBOM	ST11	0	1	TP	PCH	TN8	B13
NOBOM	ST12	0	1	TP	PCH	TP8	D13

U2B



side x2 #1 USB Debug port

Rear x4

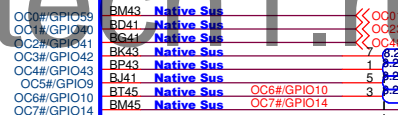
Touch Panel

CARD READER

#9 USB Debug port

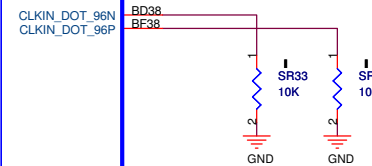
Web Cam

USB



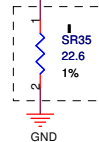
NOTE:

Used for integrated graphics, generate USB backbone,
24MHz HDA bit, and 48MHz clock.



NOTE:

trace length < 200 mils



PEGATRON DT-MB RESTRICTED SECRET

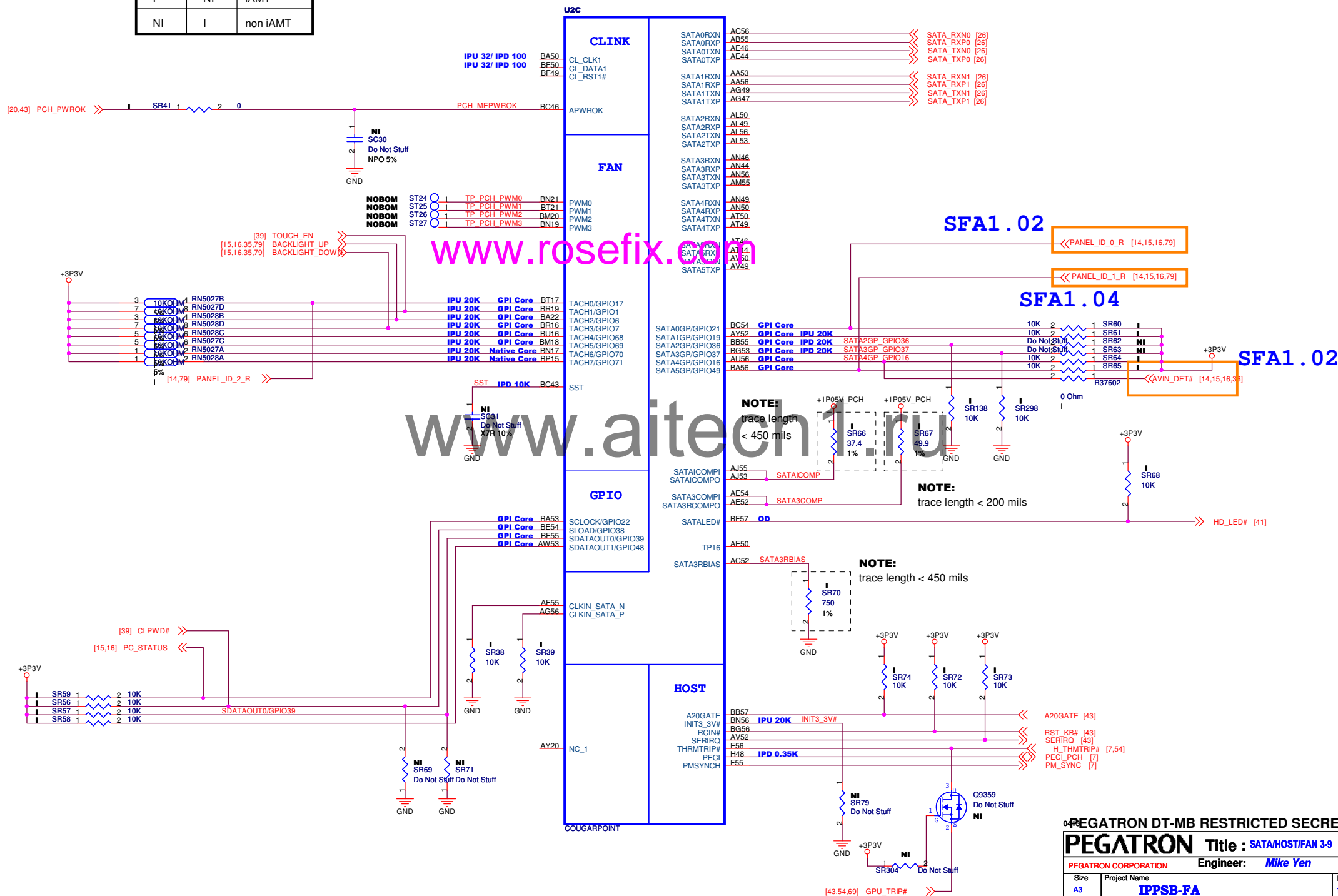
PEGATRON Title : PCIE/USB/DMI 2-9

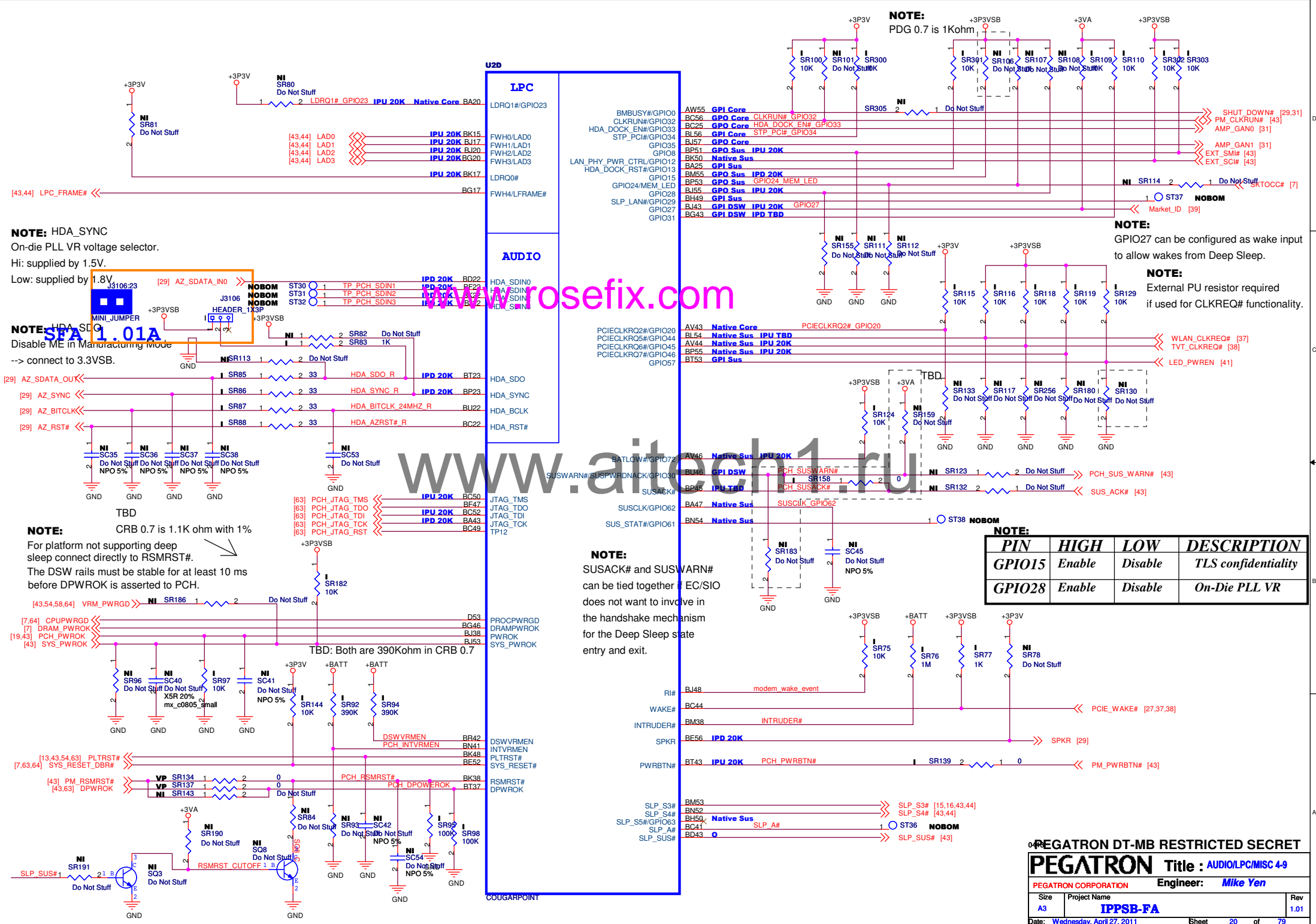
PEGATRON CORPORATION Engineer: Mike Yen

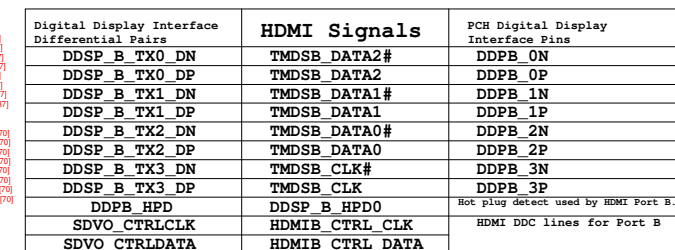
Size A3 Project Name IPPSB-FA Rev 1.01

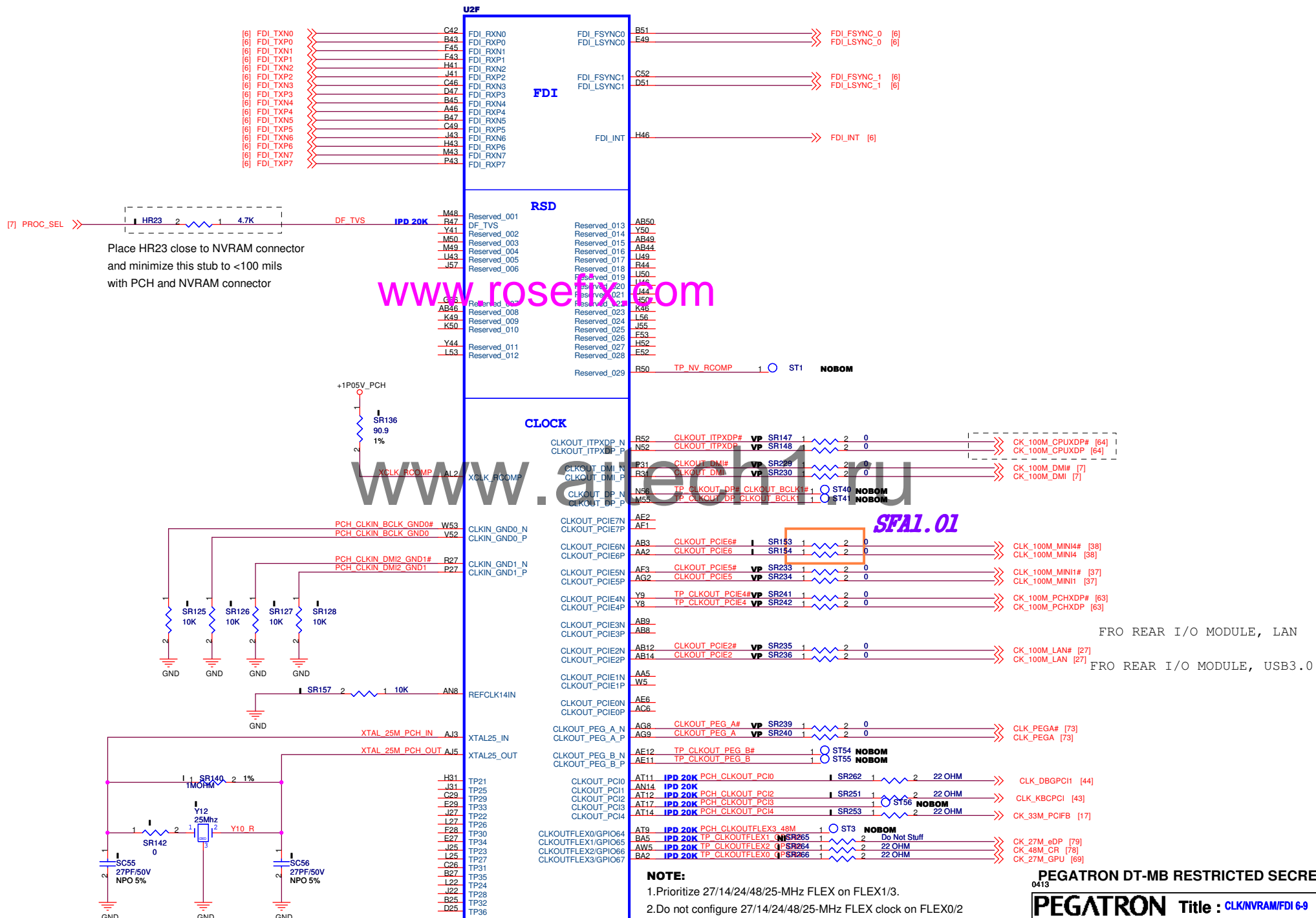
Date: Wednesday, April 27, 2011 Sheet 18 of 79

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT









NOTE:

1. Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2. Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2 if more than 2 PCI clocks + PCI loopback are routed.
3. With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3
a. 27MHz(SSC/non-SSC) b. 14.31818MHz c. 24/48 d. 25MHz

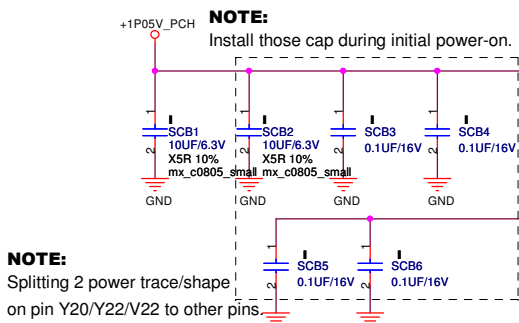
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **CLK/INVRAM/FDI 6-9**

PEGATRON CORPORATION Engineer: **Mike Yen**

Size	Project Name	Rev
A3	IPPSB-FA	1.01

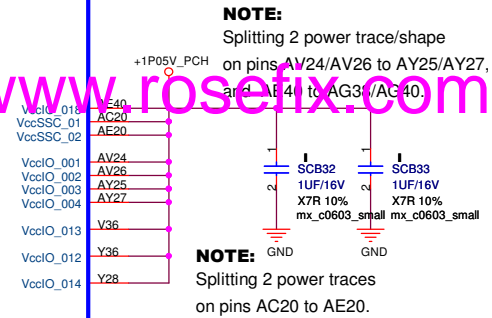
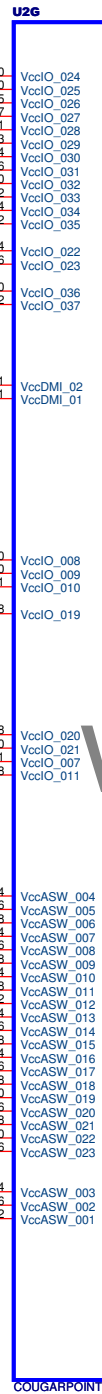
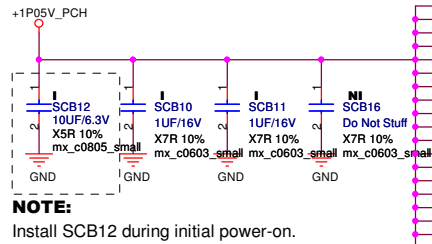
Date: **Wednesday, April 27, 2011** Sheet **22** of **79**



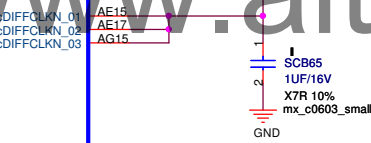
NOTE:
Splitting 2 power trace/shape on pin Y20/Y22/V22 to other pins.

NOTE:
Trace needs to be at least 20 mils width with full VSS/VCC reference plane

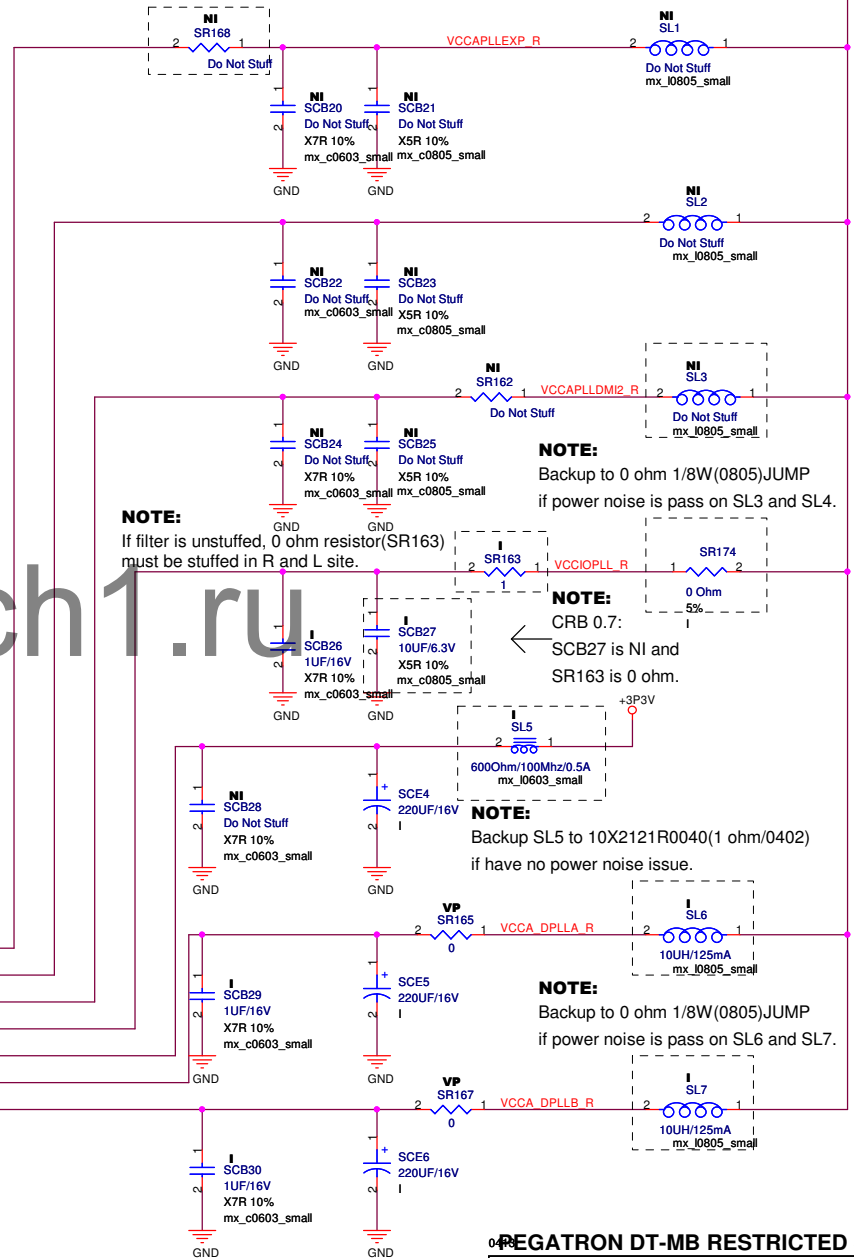
NOTE:
Splitting 2 power trace/shape



NOTE:
Splitting 2 power traces on pins AC20 to AE20.



NOTE:
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC in On-Die VR mode.



NOTE:
Place SCB59 and SCB66 near pin AU20,
SCB60 near pin AL38,
SCB61 and SCB67 near BC17.

NOTE:
Splitting 2 power trace/shape on
pin AV20/AU20 and AU22.

NOTE:
Install SCB58 during initial power-on.

NOTE:
NI or install is decided to DSW support or not.

NOTE:
Install SCB31 during initial power-on.

NOTE:
Splitting 2 power trace/shape on
pin AV28, AY31/AY33, and AV30/AV32.

NOTE:
Place SCB53 near pin BT35, SCB54 near pin U31,
and SCB69 near pin AV30/AT40.

NOTE:
Place SCB56 near PCH within 40mils.

NOTE:
Just for measurement.

CRB 0.7 is 1uF

COUGARPOINT

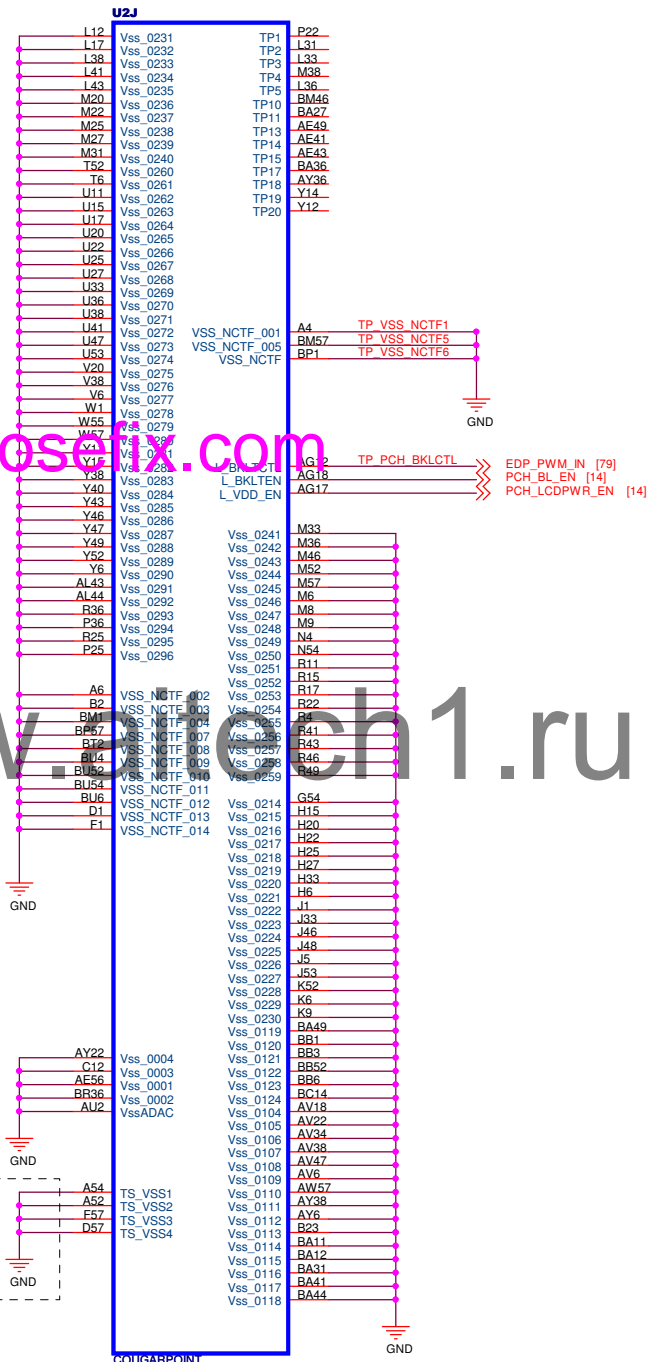
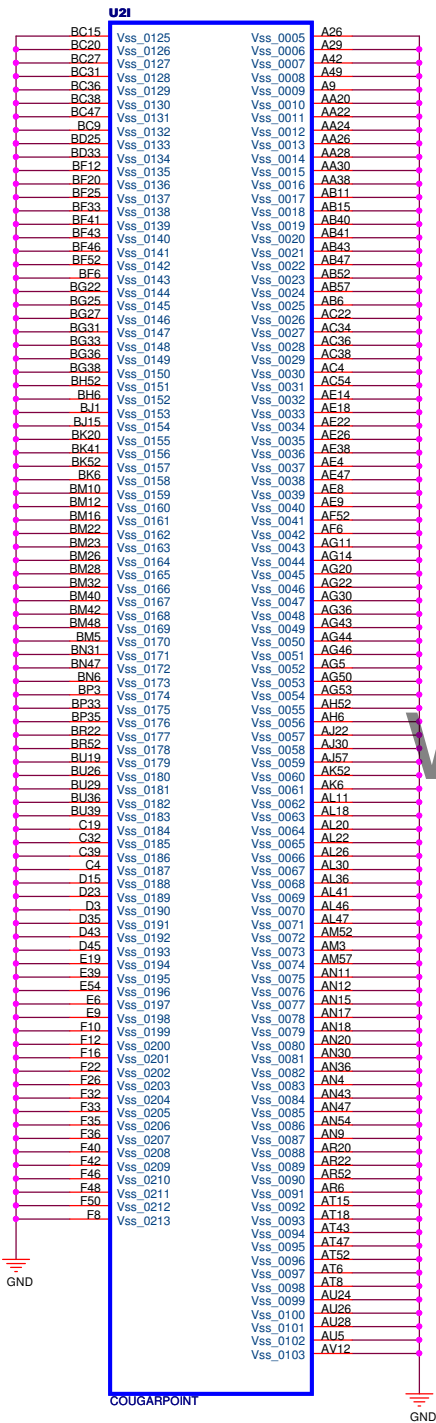
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **VCCSUS 8-9**

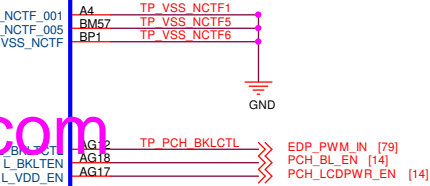
PEGATRON CORPORATION Engineer: **Mike Yen**

Size A3 Project Name **IPPSB-FA** Rev 1.01

Date: Tuesday, April 26, 2011 Sheet 24 of 79



NOTE:
BOM option depend on thermal result



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VSS 9-9

PEGATRON CORPORATION Engineer: Mike Yen

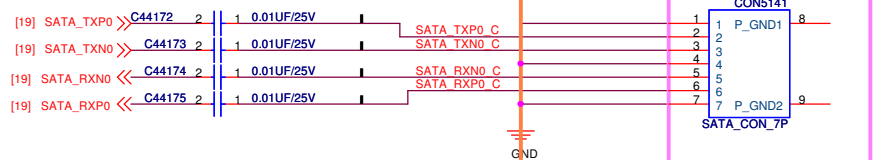
Size	Project Name	Rev
A3	IPPSB-FA	1.01

Date: Wednesday, April 27, 2011 Sheet 25 of 79

已更改完成

SATA HDD CON

1.01 20101019 revised



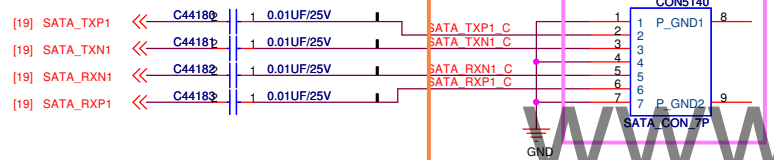
SATA CONTROLLER #1
(MASTER)

COLOR = DARK BLUE

www.rosefix.com

SATA ODD CON

1.01 20101019 revised

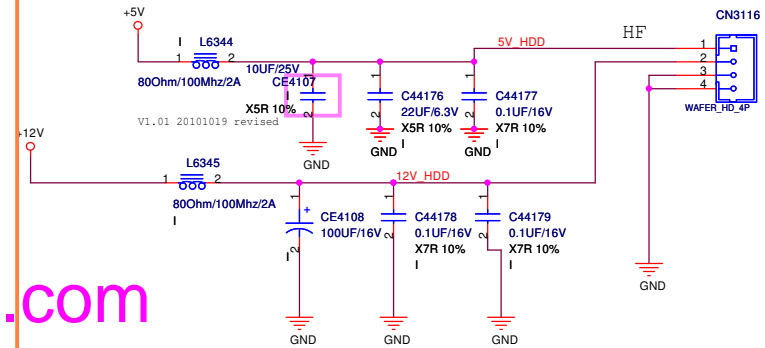


SATA CONTROLLER #2
(SLAVE)

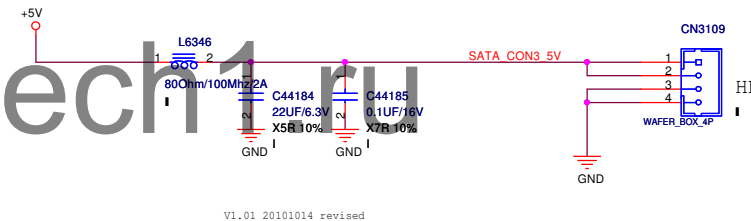
COLOR = WHITE

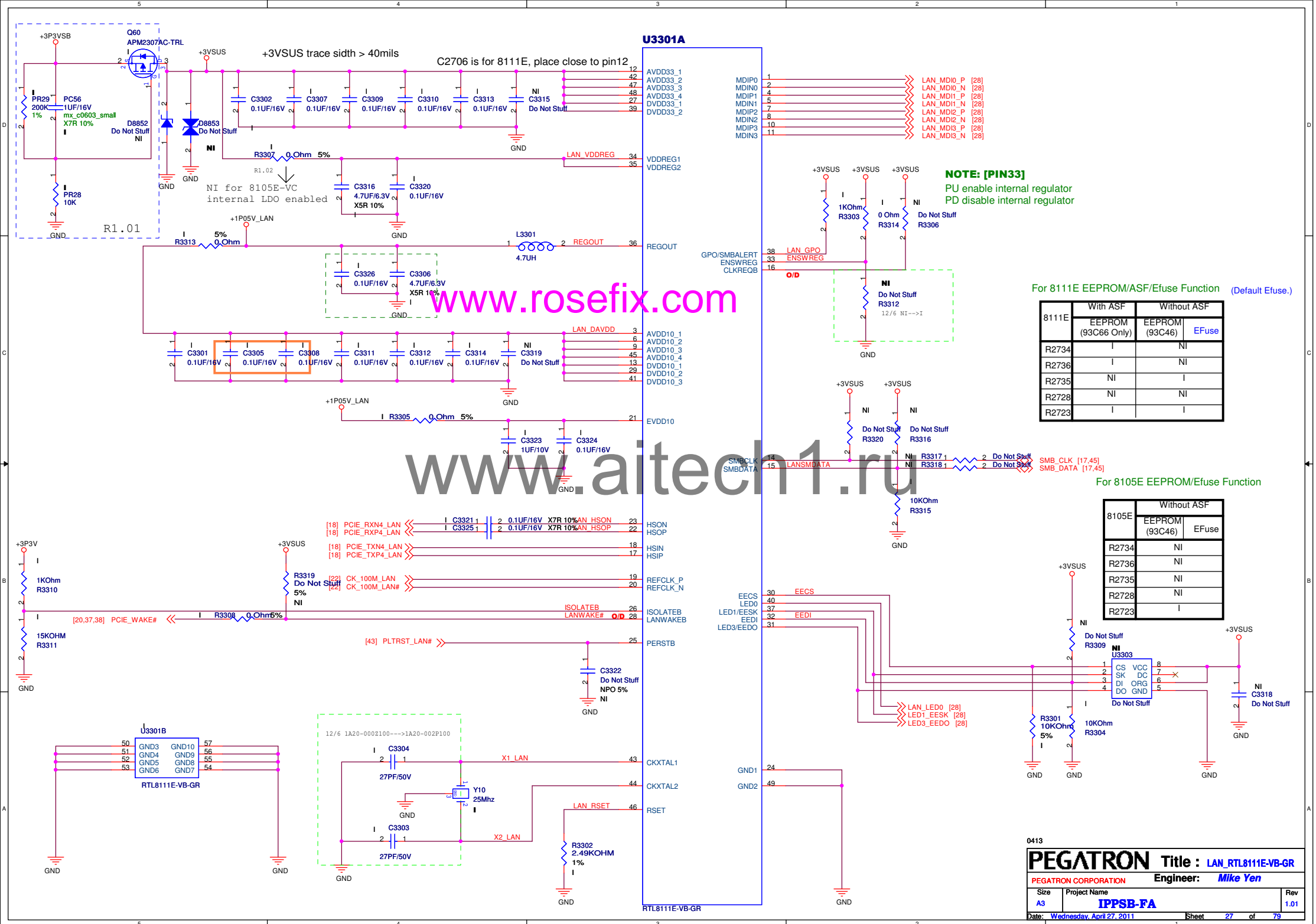
www.aitech1.ru

SATA POWER CONN.

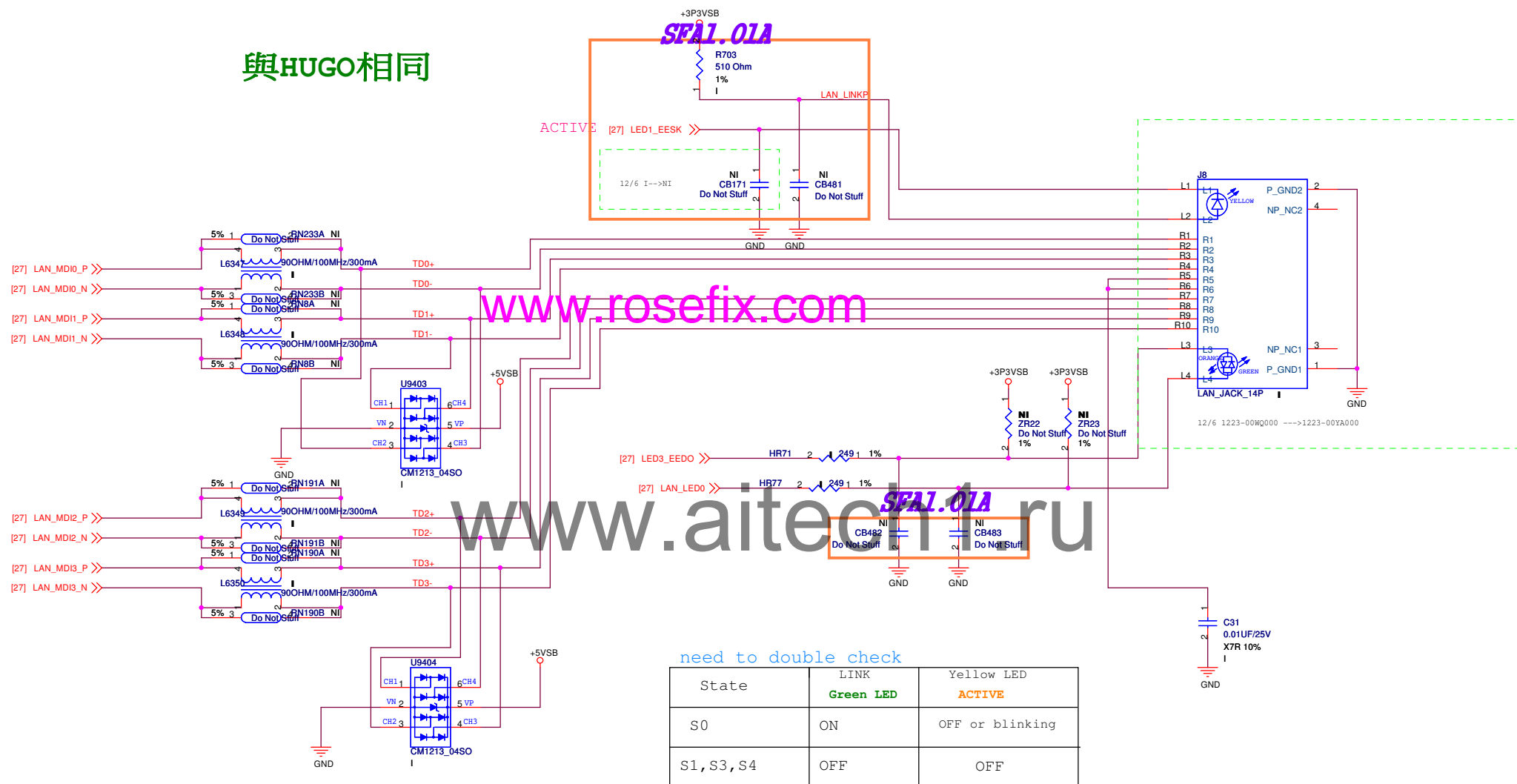


ODD POWER CONN.



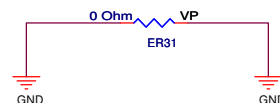


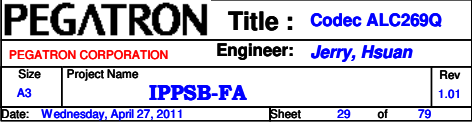
與HUGO相同



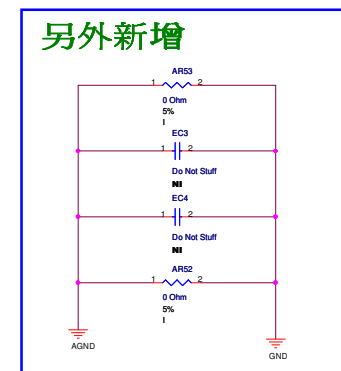
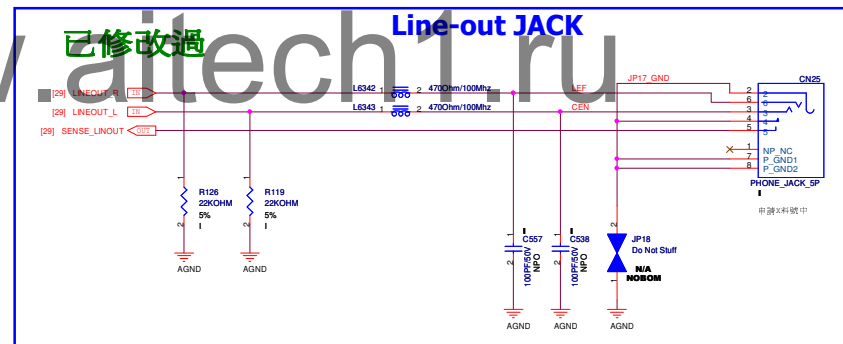
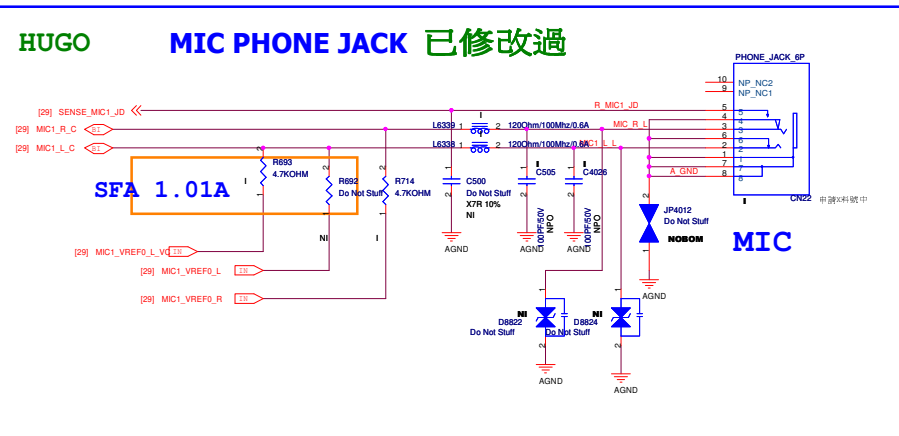
need to double check

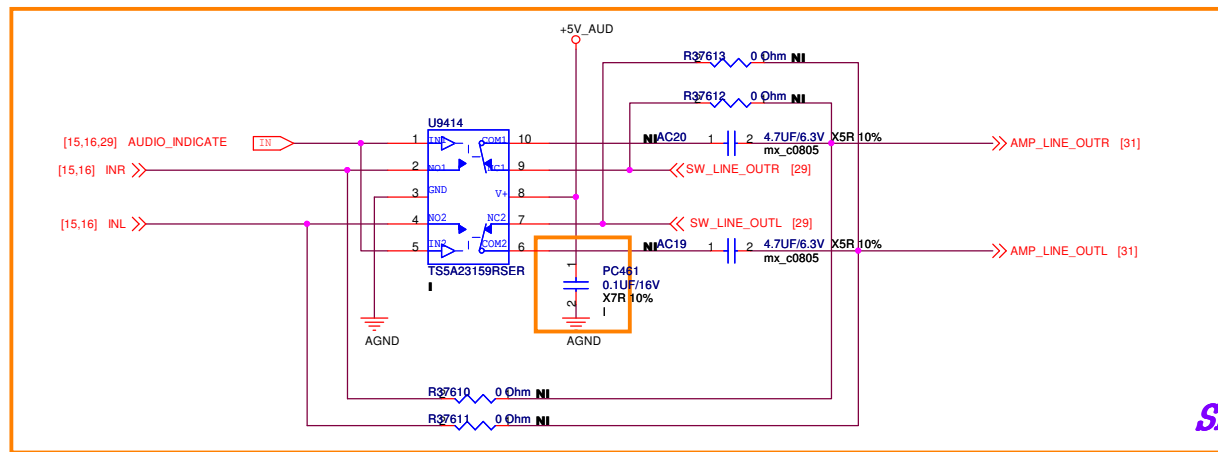
State	LINK Green LED	Yellow LED ACTIVE
S0	ON	OFF or blinking
S1,S3,S4	OFF	OFF





www.aitech1.ru



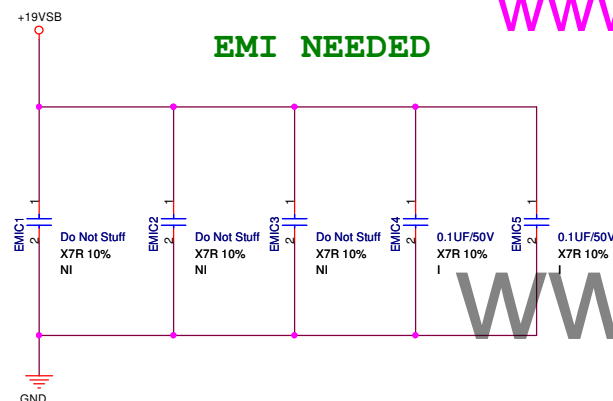


SFA1.04

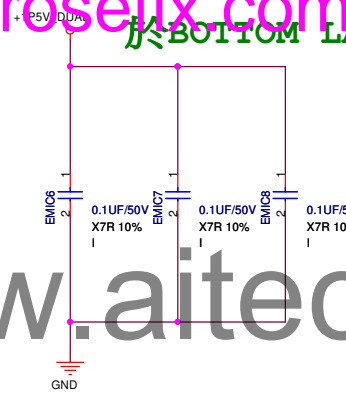
www.rosefix.com

於BOTTOM LAYER 上

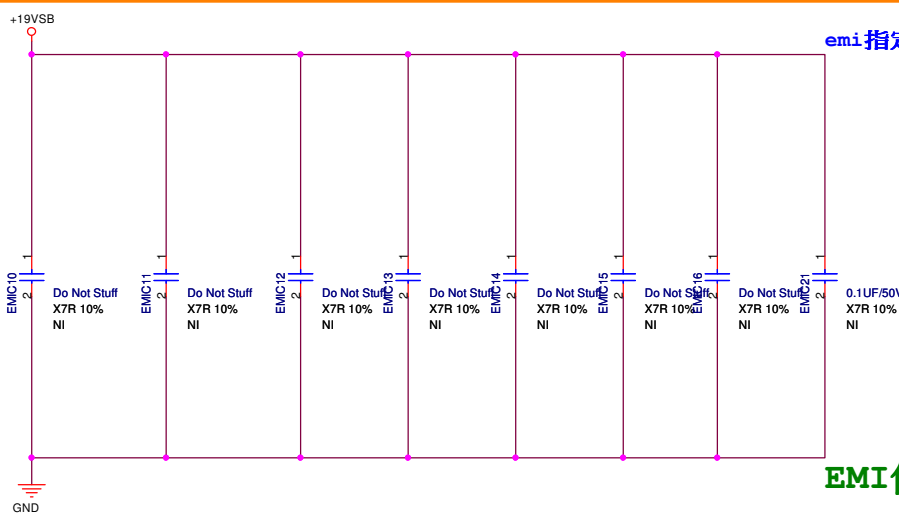
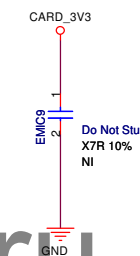
於TOP LAYER 上



EMI NEEDED

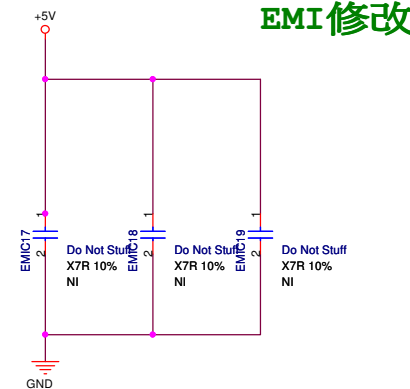


www.aitech1.ru

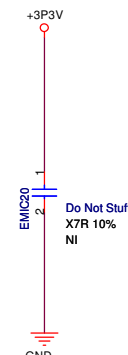


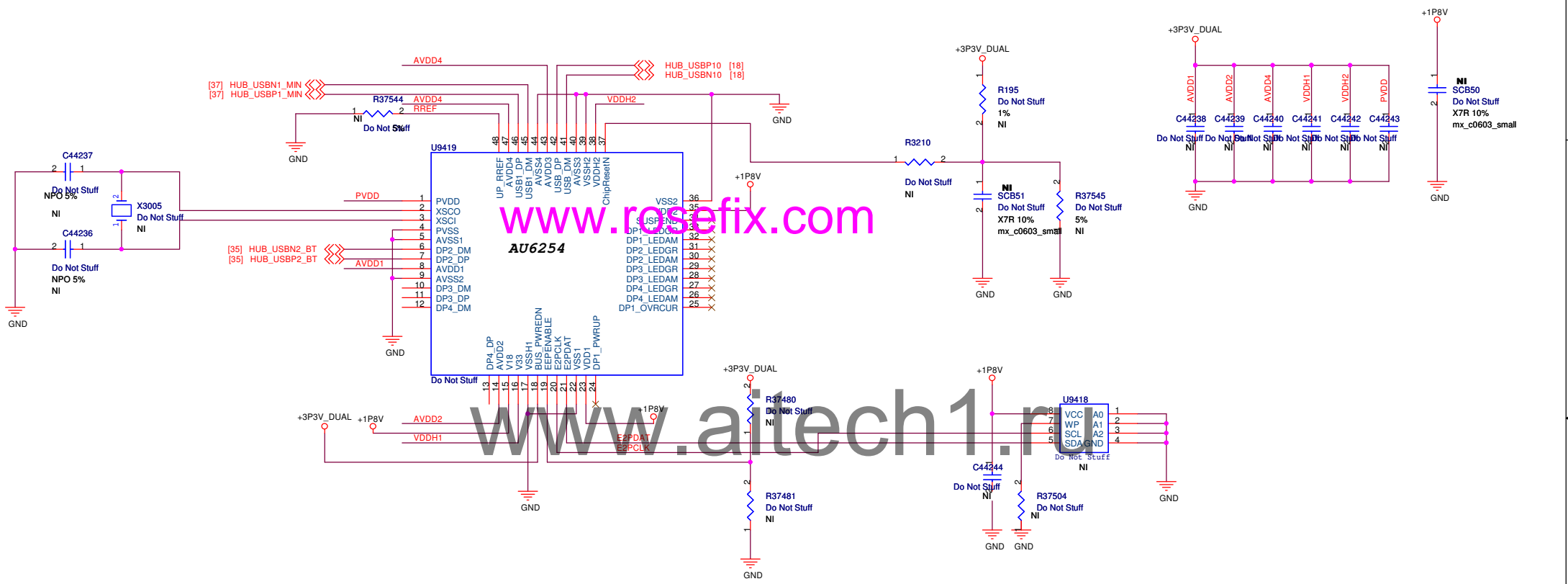
emi指定位置

EMI修改



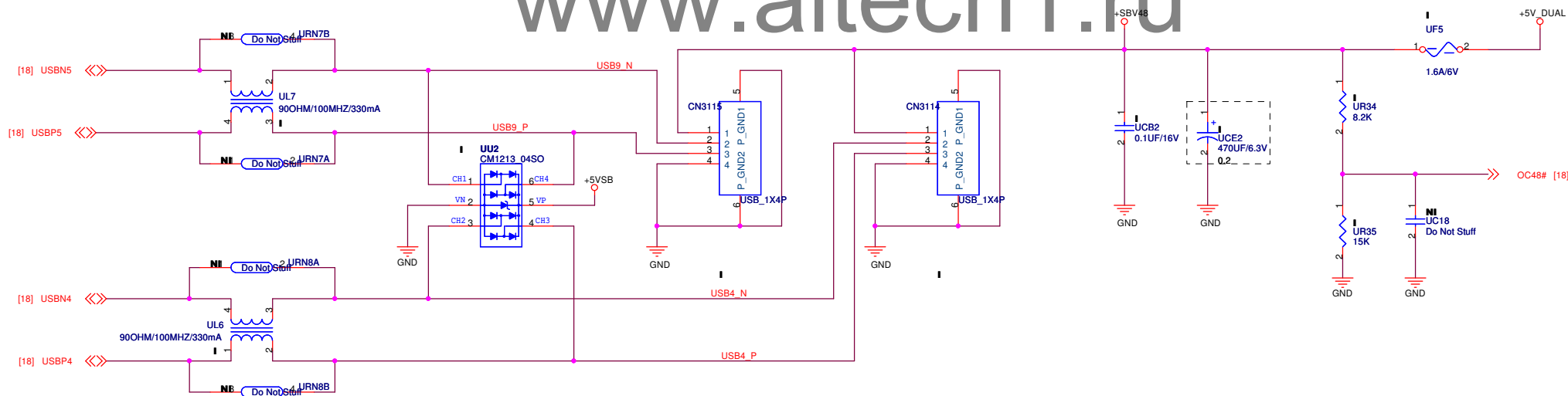
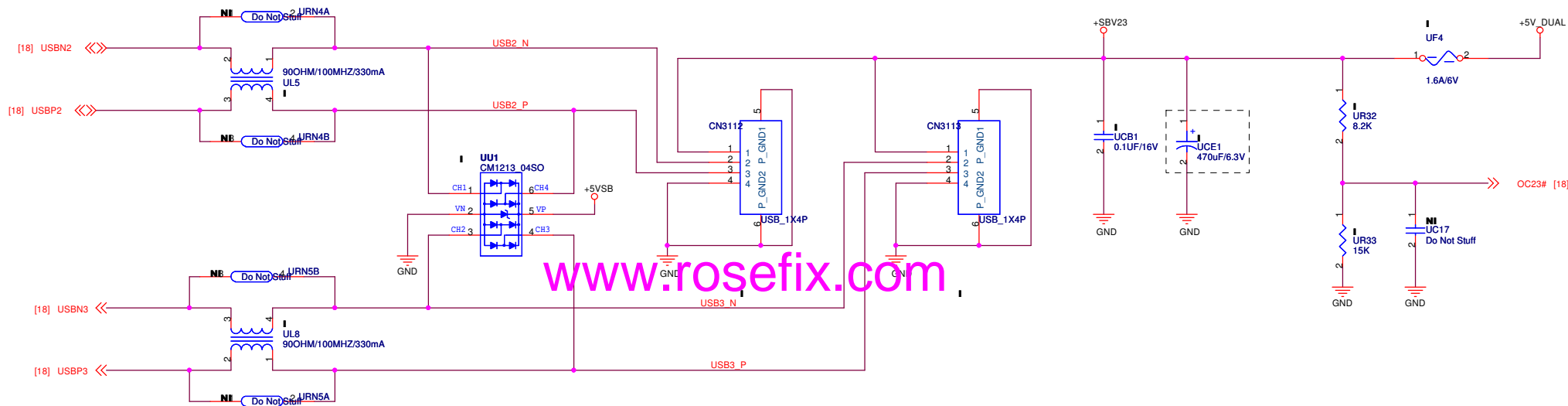
EMI修改



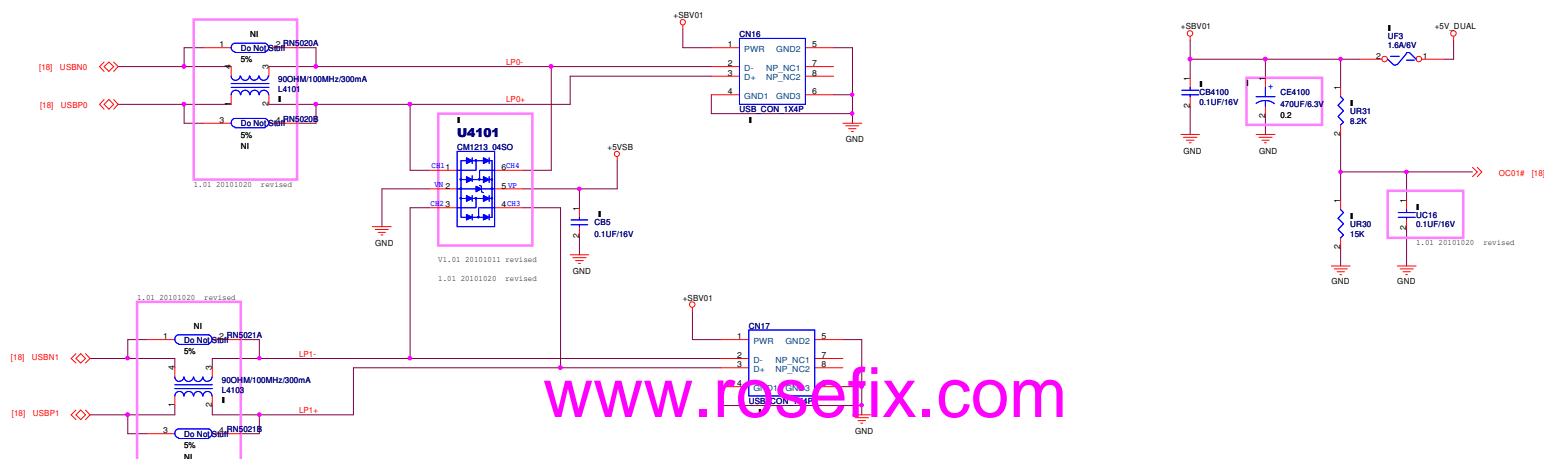


整頁修改過

Rear USB2.0 *4

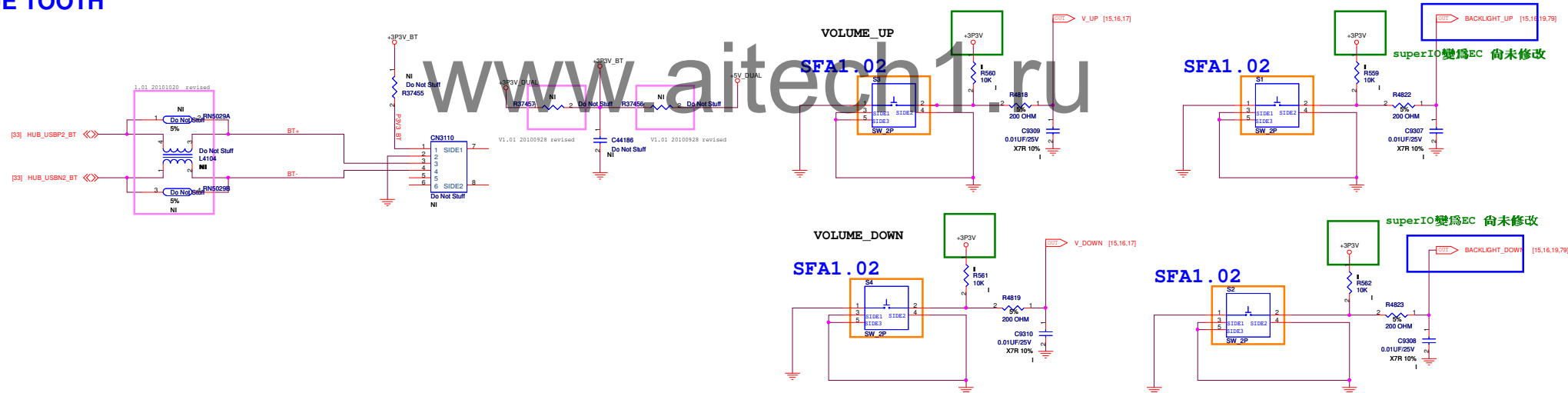


已修改過

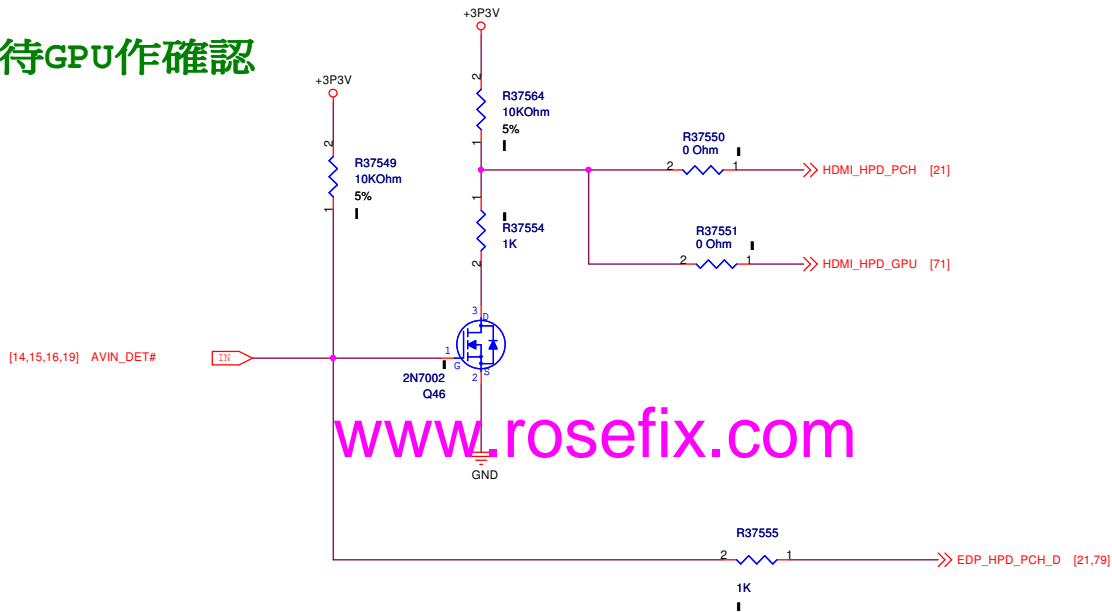


另外增加
Internal I/O
BLUE TOOTH

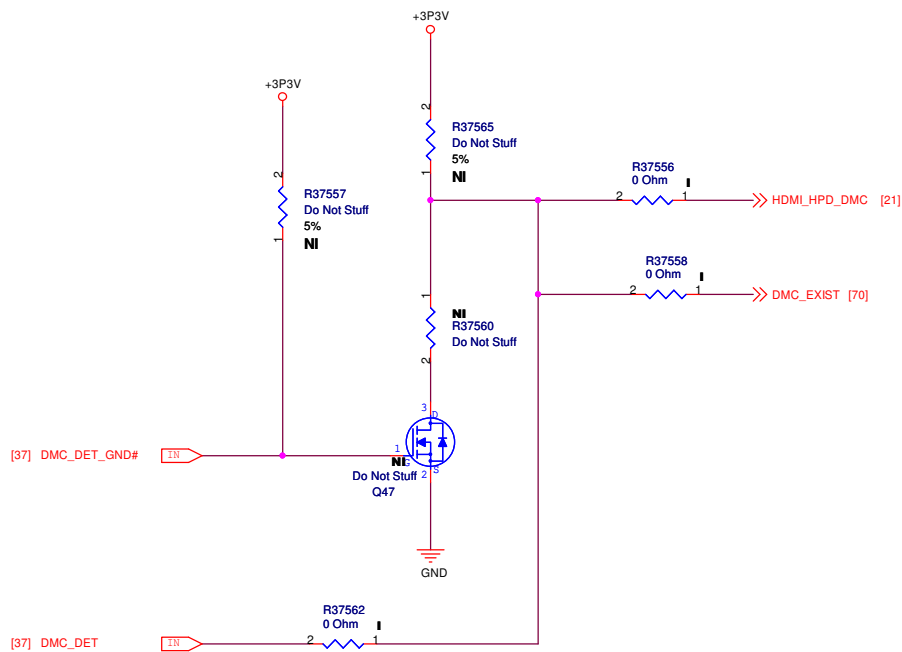
the DMC device connected BT symbols is needed



待GPU作確認

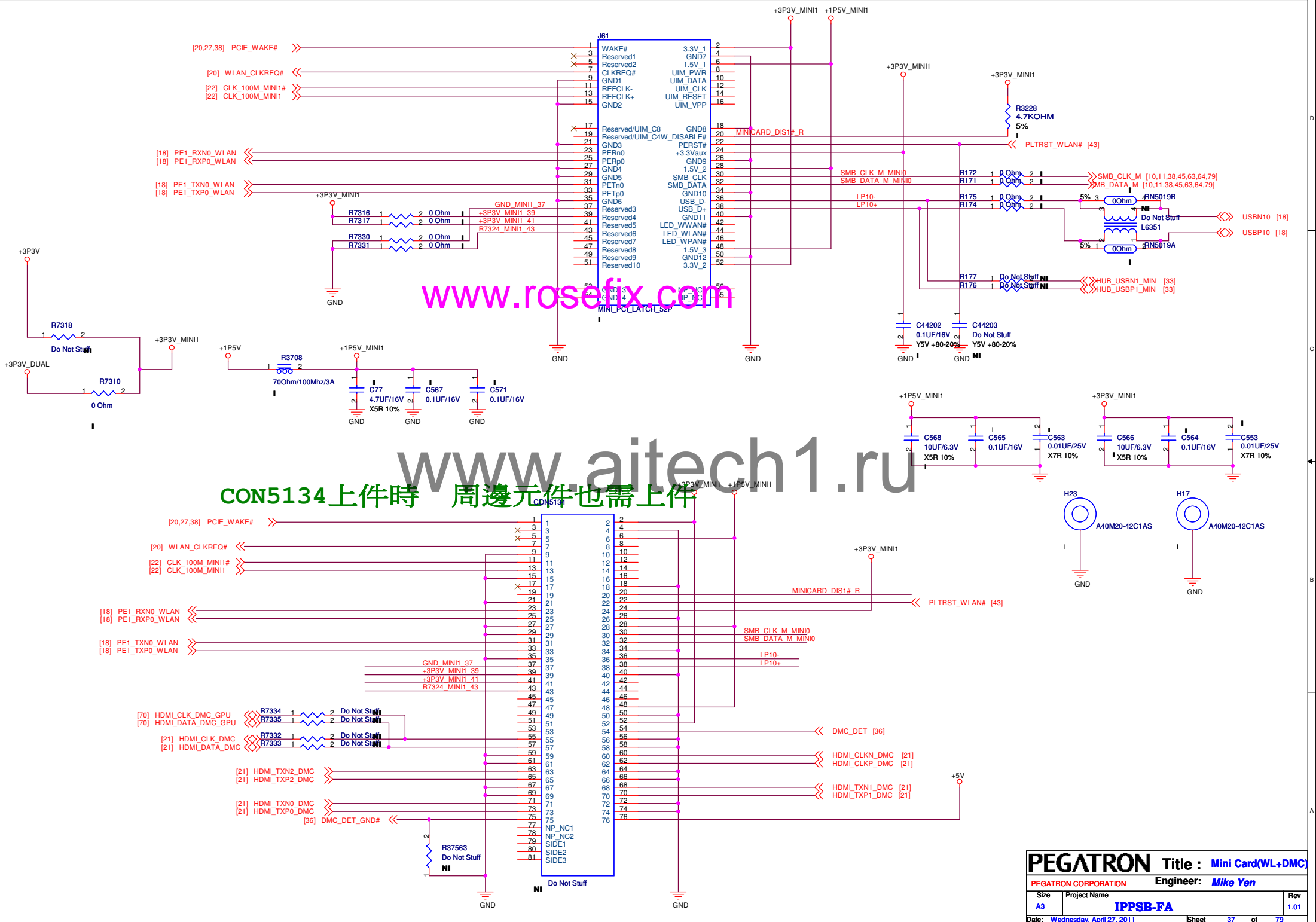


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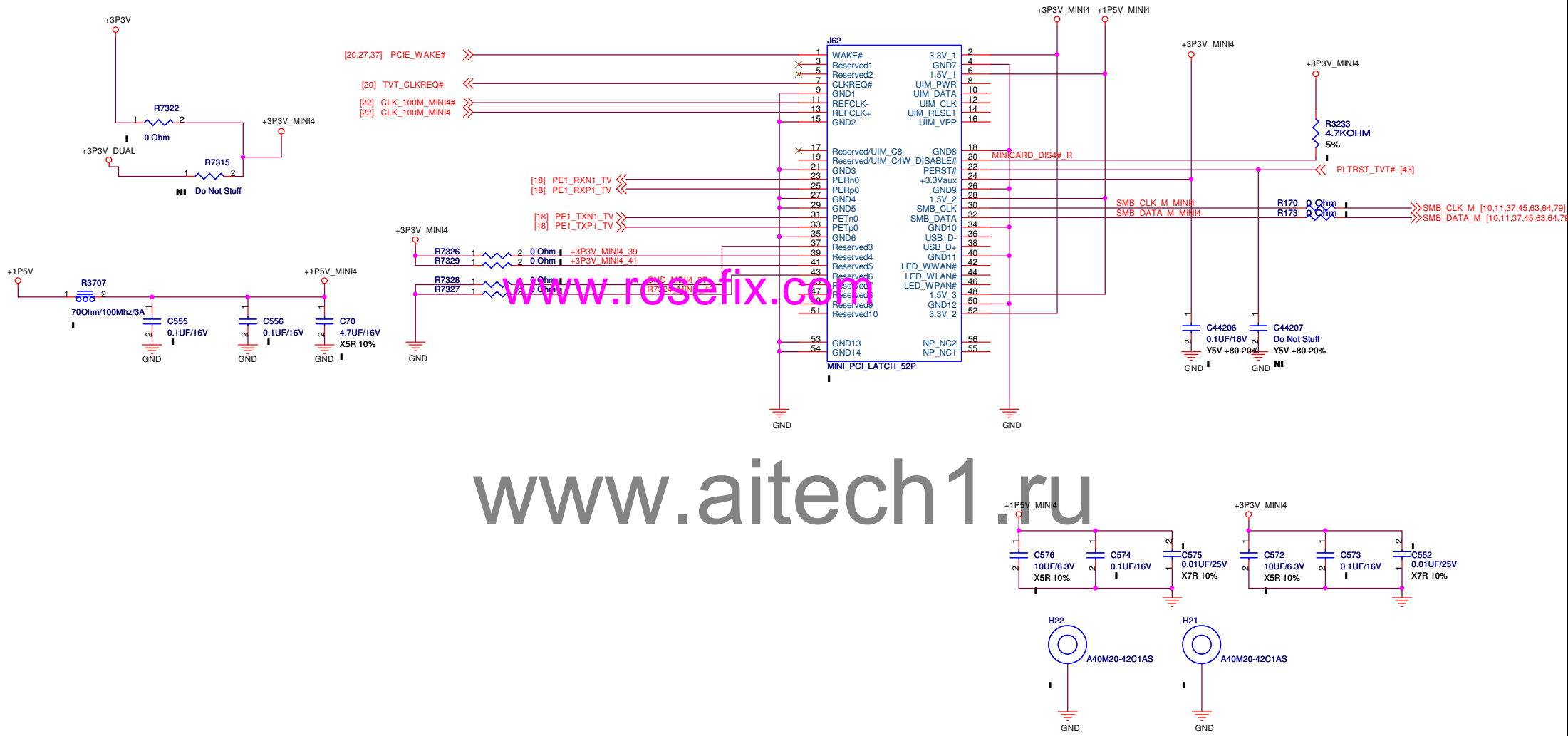


0413

PEGATRON		Title : HPD DET	
R&D 2		Engineer: Jerry, Hsuan	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet	36 of 79



CON5134上件時 周邊元件也需上件

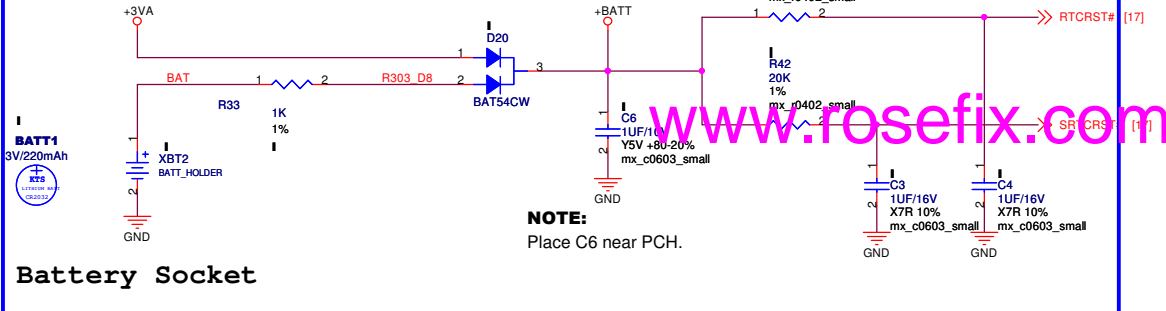


CLR CMOS CIRCUIT

CLR PASSWORD CIRCUIT

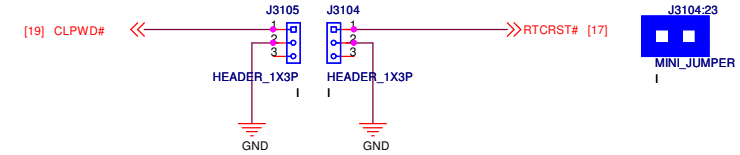
更換SCOTT的

External RTC Circuitry



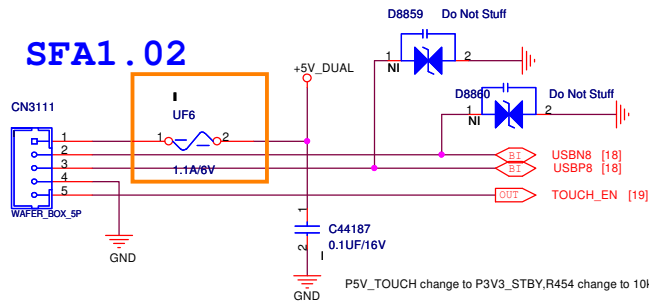
PASSWORD	
1-2	CLEAR
2-3	Default

CMOS RTC	
1-2	CLEAR
2-3	Default



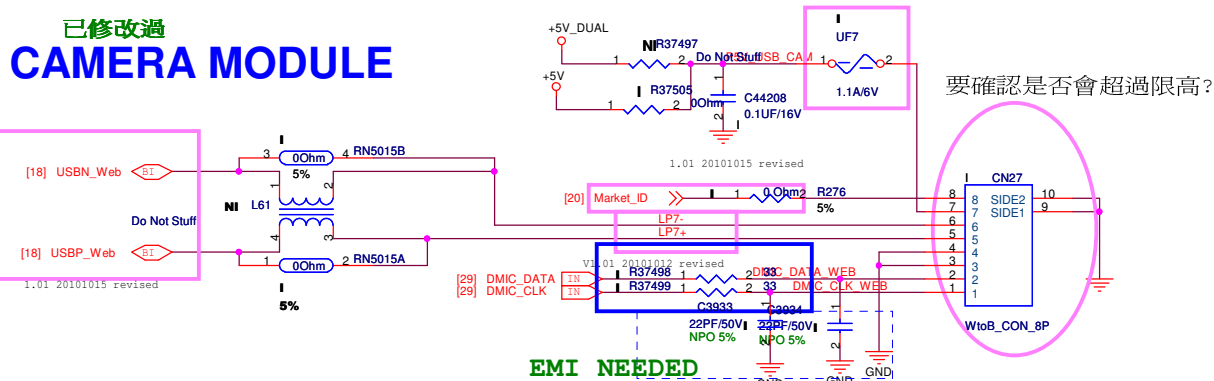
TOUCH

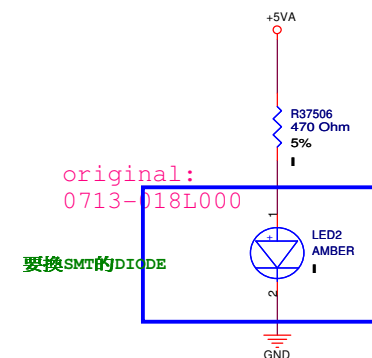
SFA1.02



SFA1.03

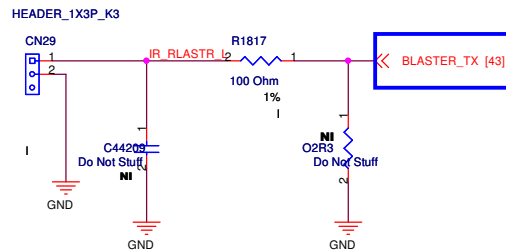
已修改過 CAMERA MODULE





線條未改

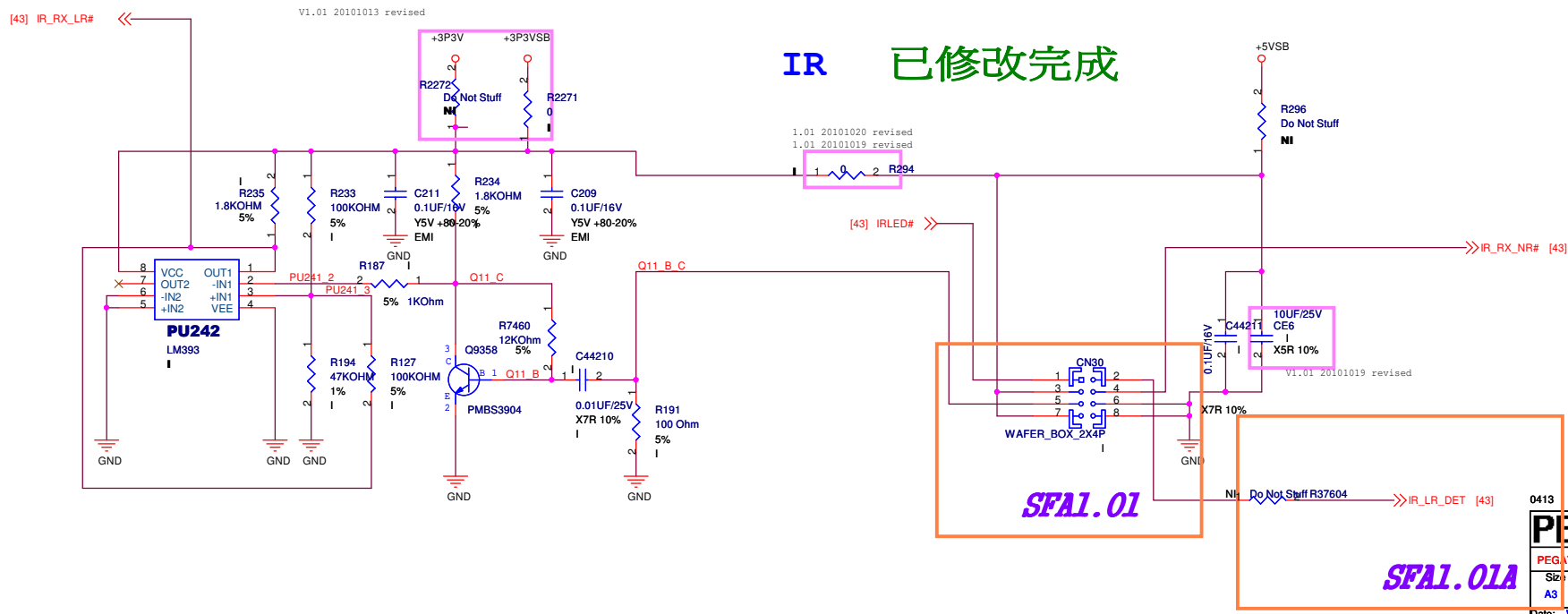
IR Blaster



www.rosefix.com

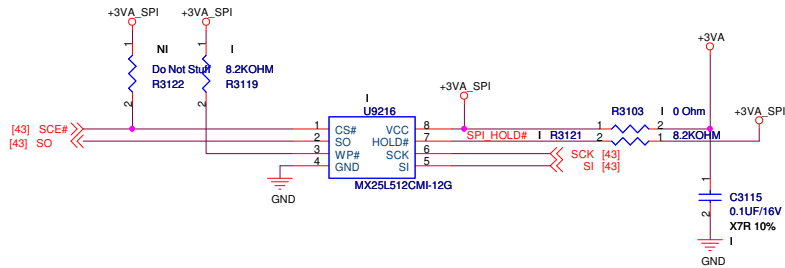
www.aitech1.ru

IR 已修改完成



Date: Wednesday, April 27, 2011 Sheet 43 of 79

SPI ROM+ External programming conn.



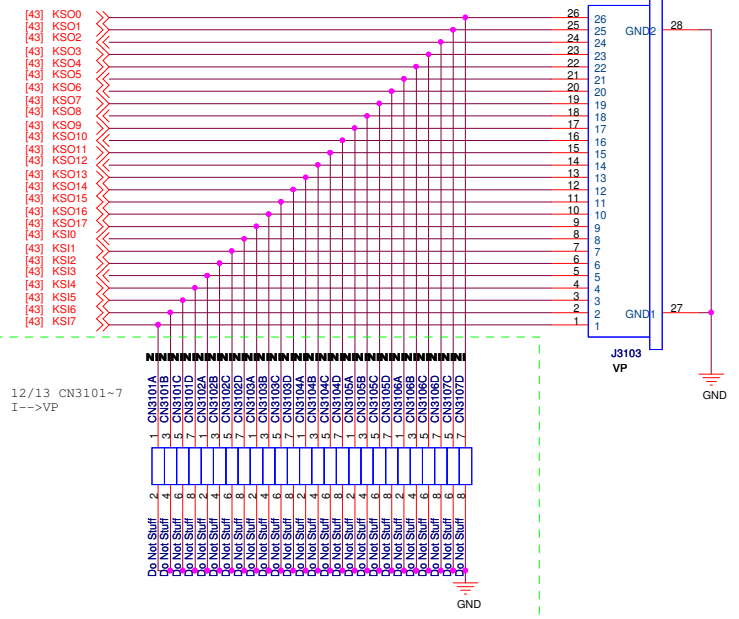
Touch PAD(deleted)

For Instant Key & Switch

Note: Close to EC

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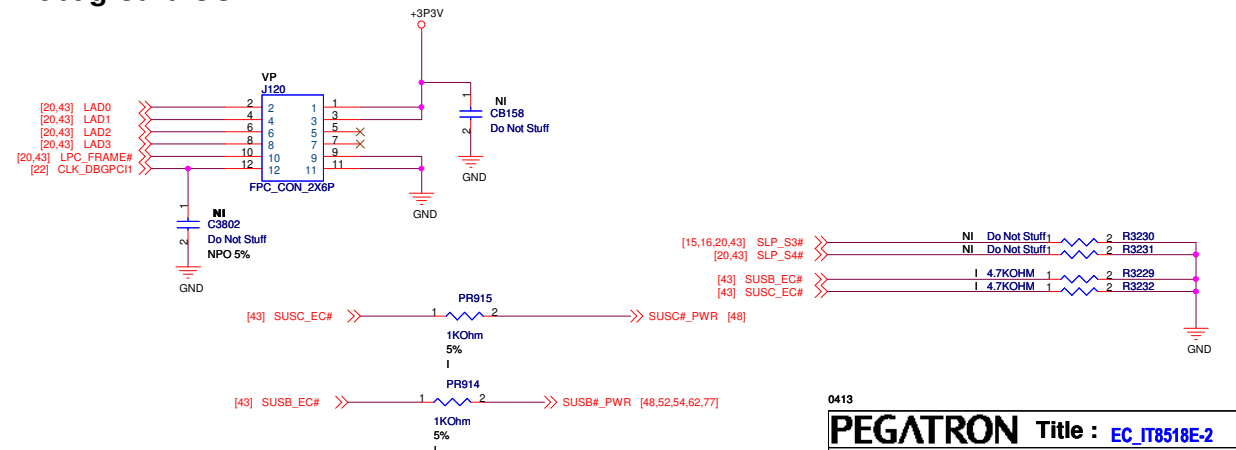
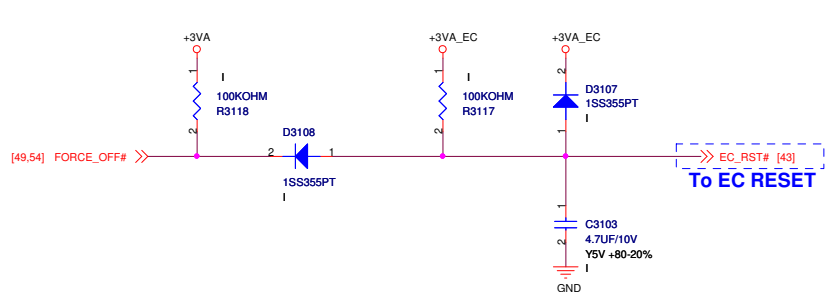
Keyboard Connector(debug)



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For EC PU/PD

Debug Card CON



0413

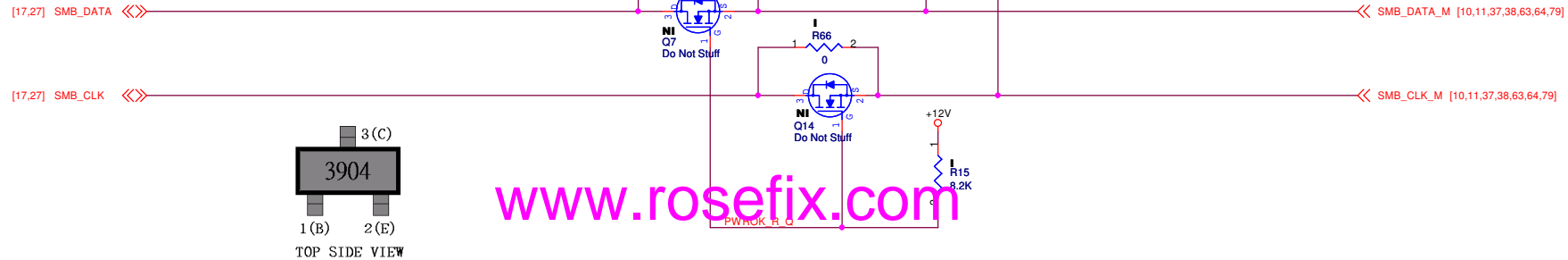
PEGATRON Title : **EC_IT8518E-2**
PEGATRON CORPORATION Engineer: **Muller_Lu**

Size Project Name
Custom **IPPSB-FA**

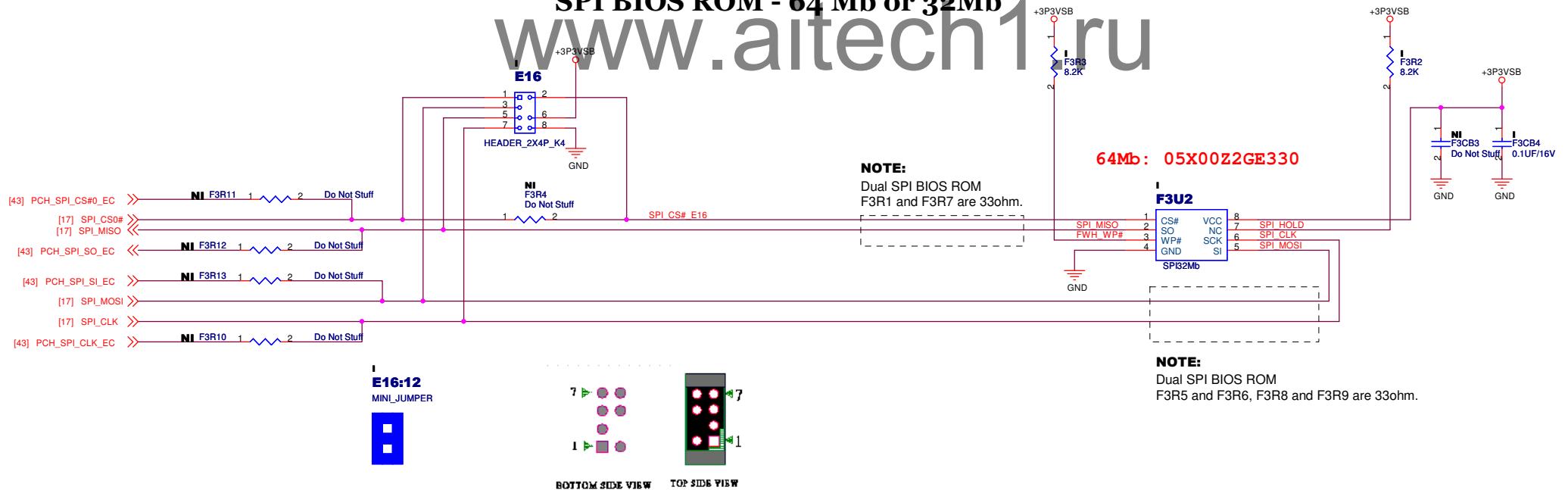
Date: Wednesday, April 27, 2011 Sheet 44 of 79

SM BUS Control

To PCH, PCI, and PCIE Slot



SPI BIOS ROM - 64 Mb or 32Mb



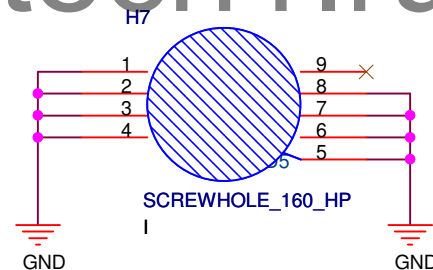
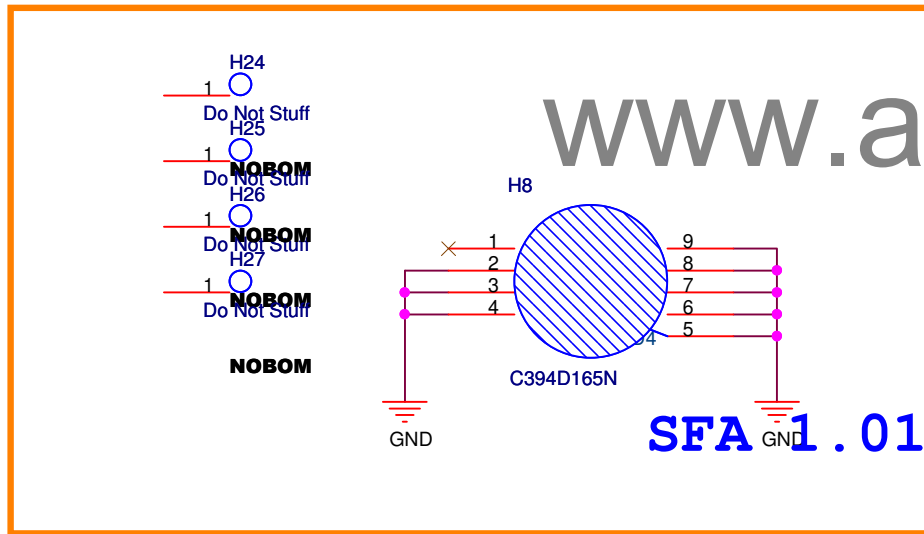
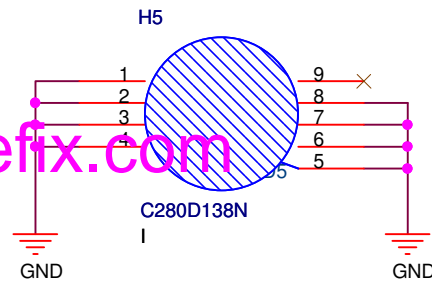
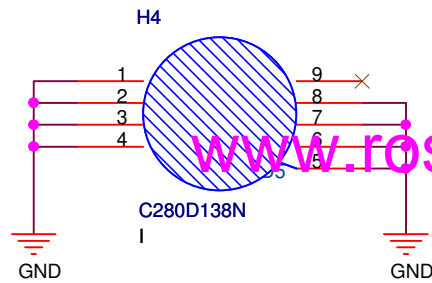
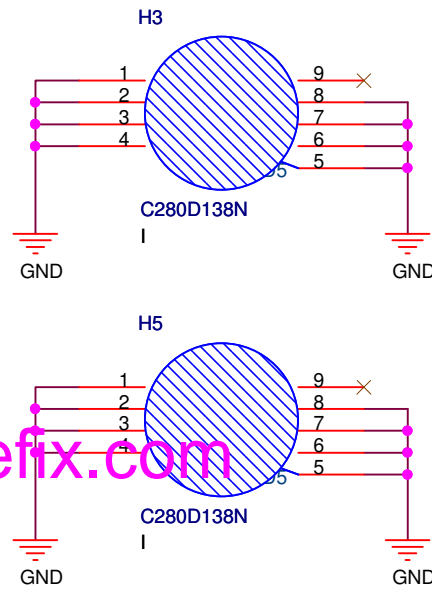
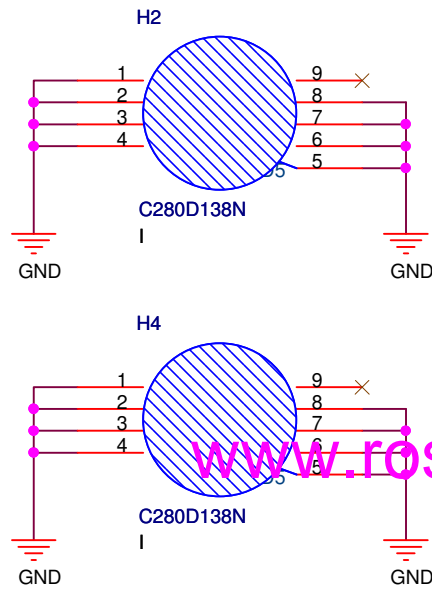
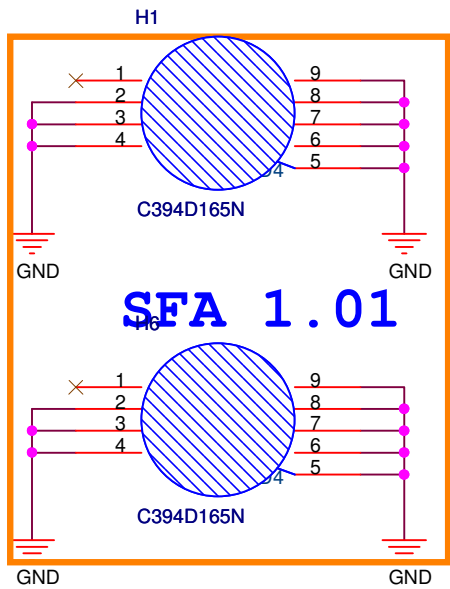
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SM BUS & SPI ROM

PEGATRON CORPORATION Engineer: XXXX-XX

Size A3	Project Name IPPSB-FA	Rev 1.01
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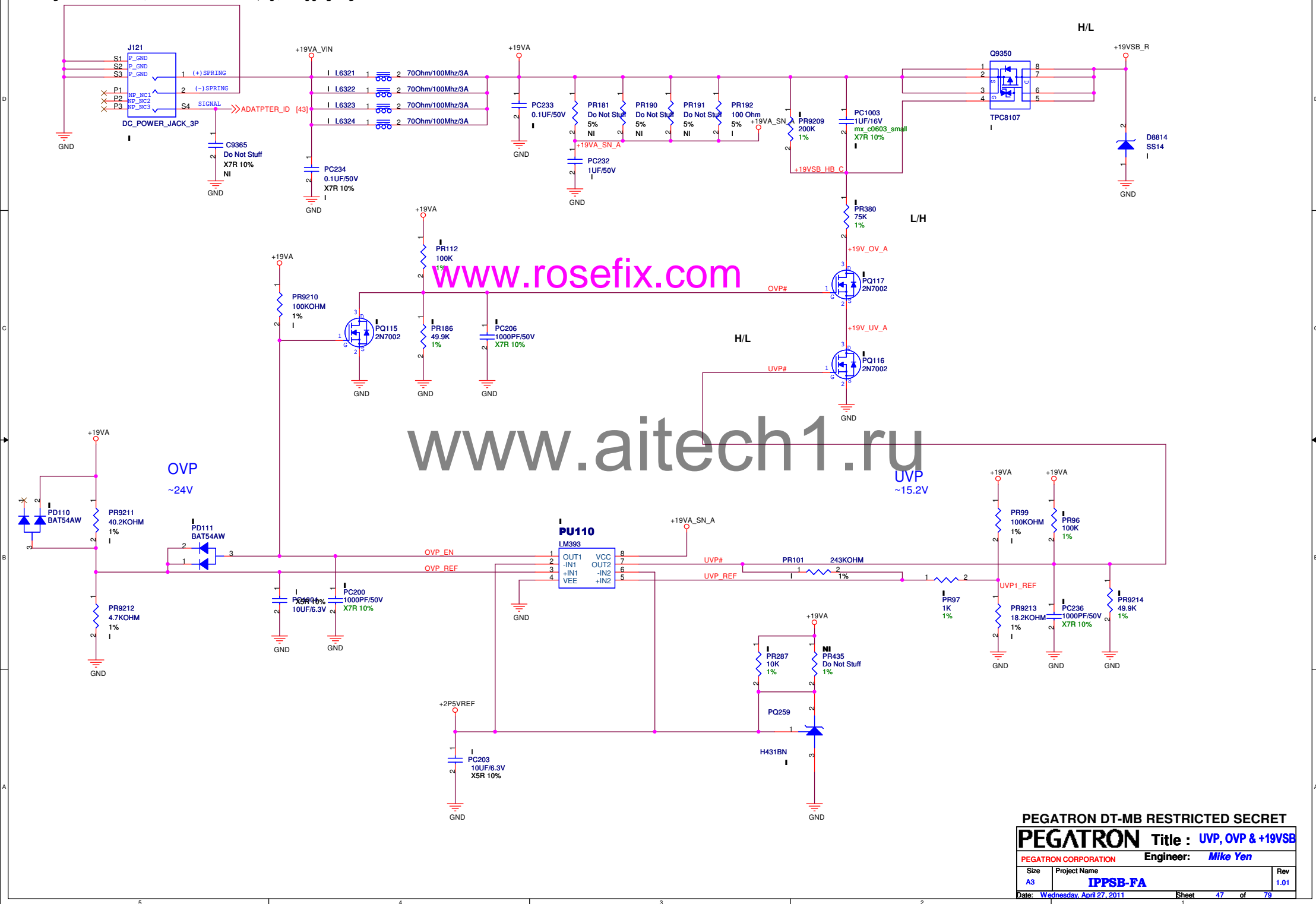
Date: Wednesday, April 27, 2011 Sheet 45 of 79

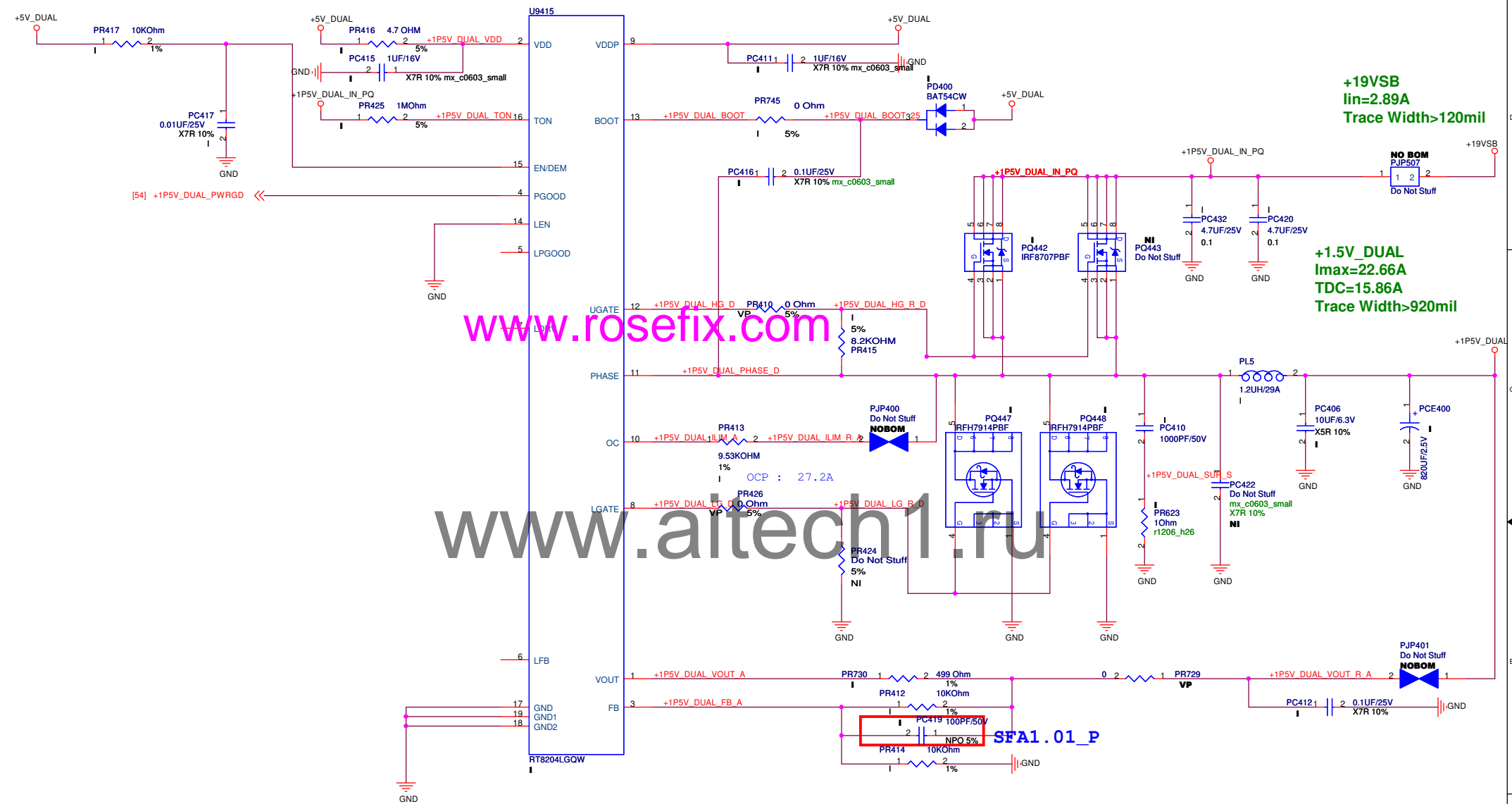


0413

PEGATRON		Title : SCREW HOLE
PEGATRON CORPORATION		Engineer: Mike Yen
Size A	Project Name IPPSB-FA	Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 46 of 79

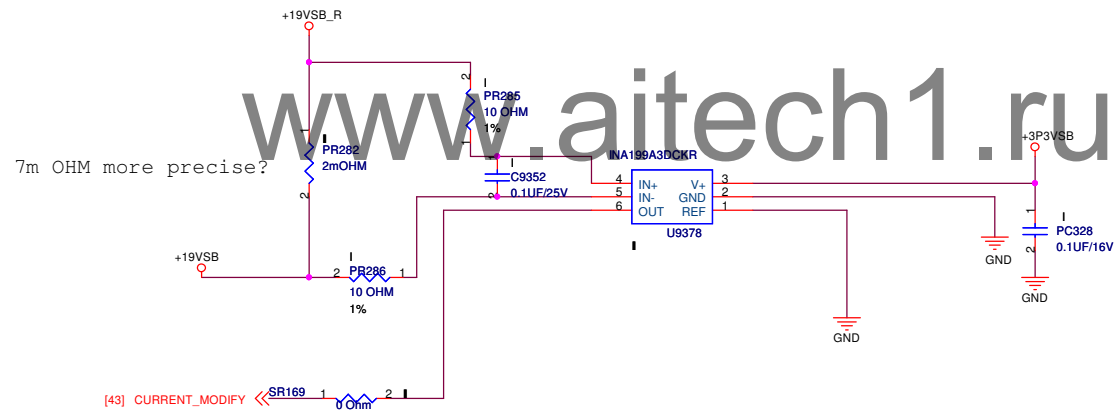
change to SIMULA /AJ261B-Y090-42F, p/n applying....

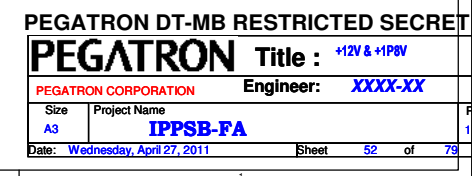


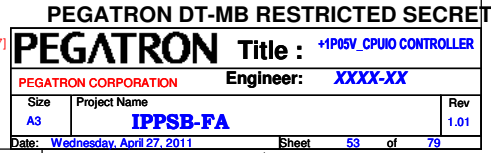


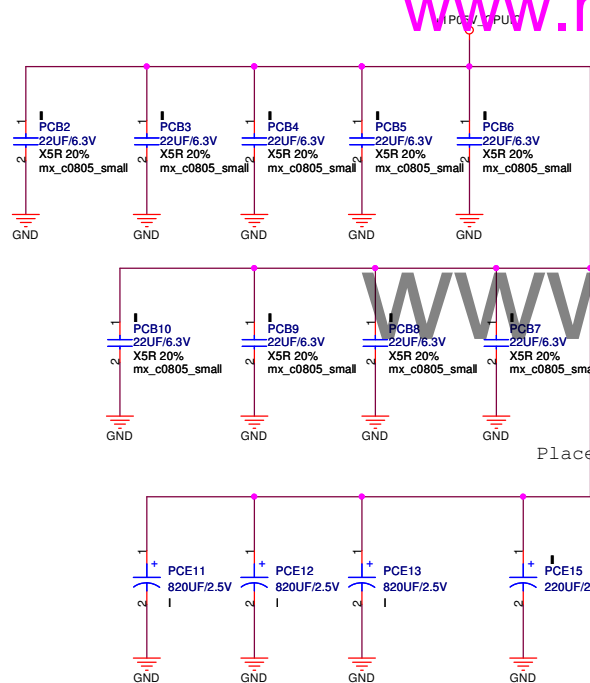
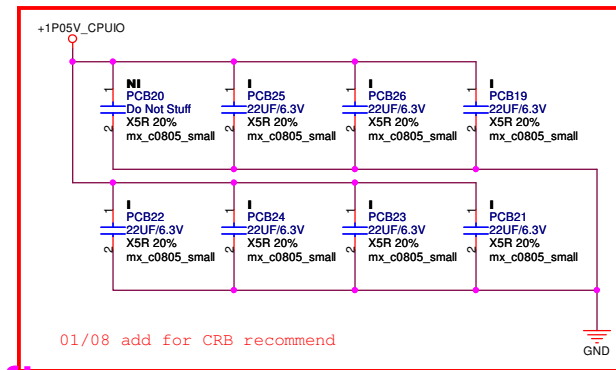
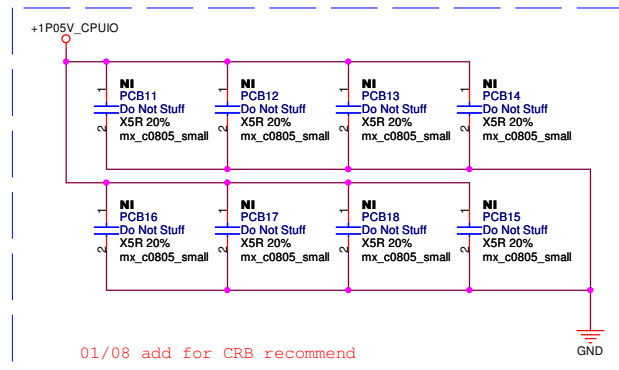
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VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2, 3
0805 placeholders	16				Backside	

Place close to CPU bottom side

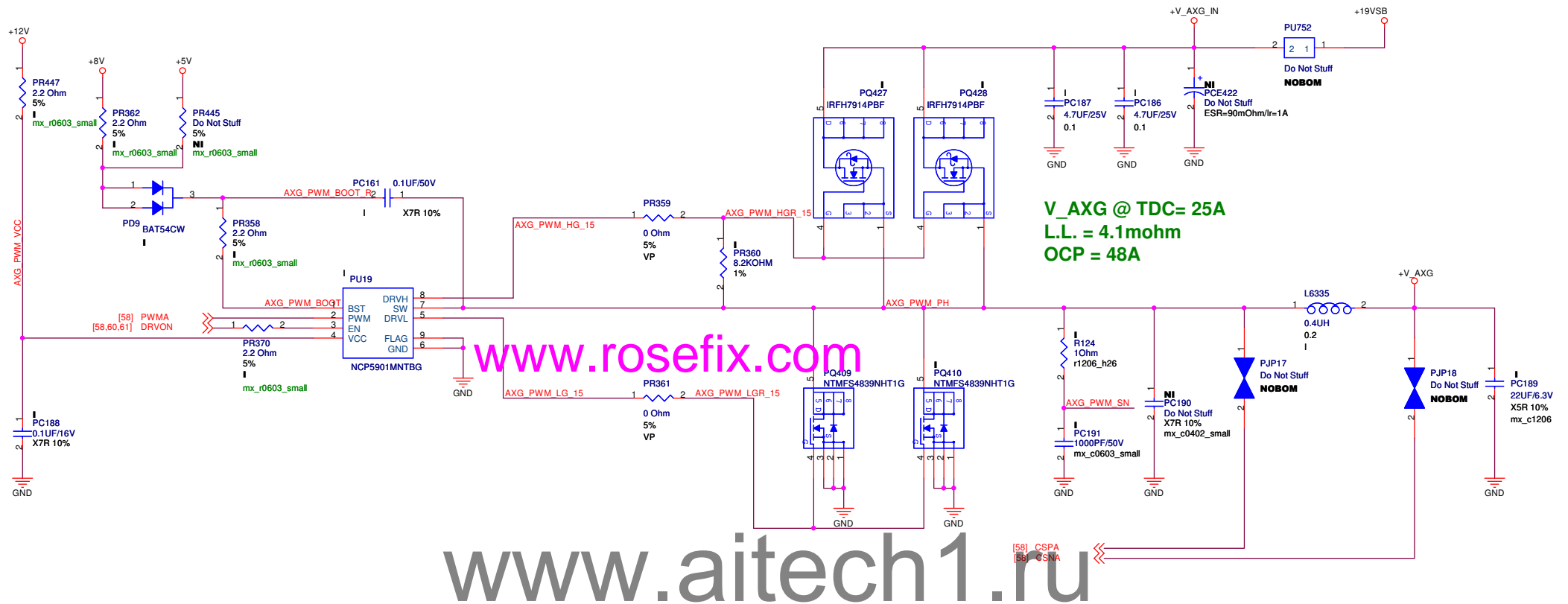
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 1P05V_CPUIO CAP

PEGATRON CORPORATION Engineer: XXXX-XX

Size A3 Project Name IPPSB-FA Rev 1.01

Date: Tuesday, April 26, 2011 Sheet 55 of 79

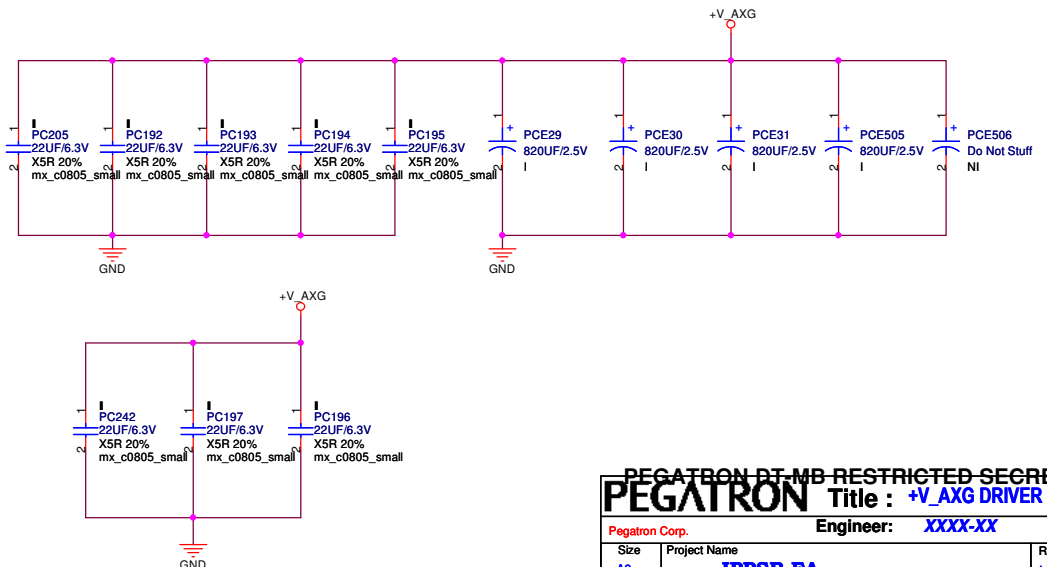


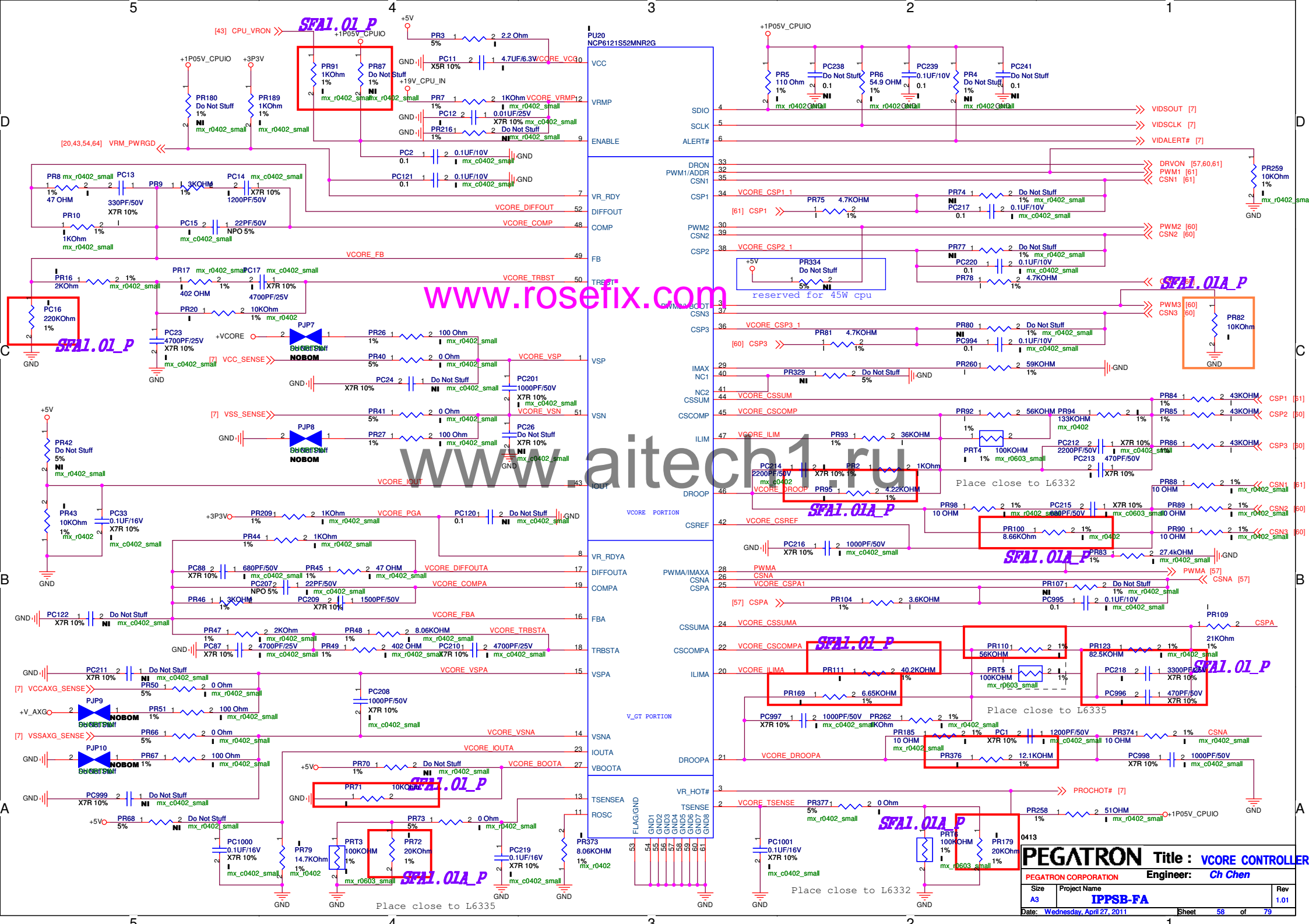
Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6



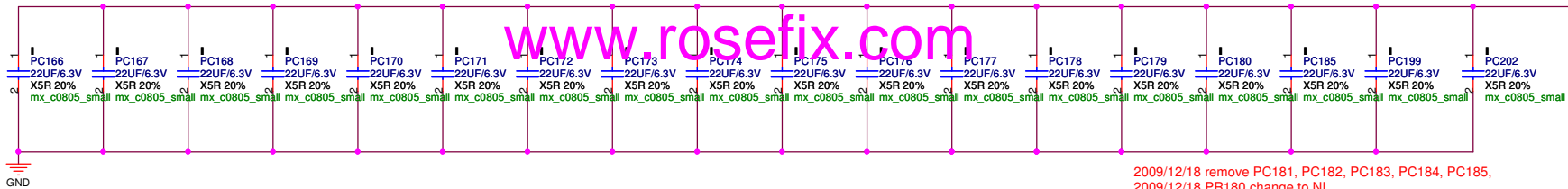
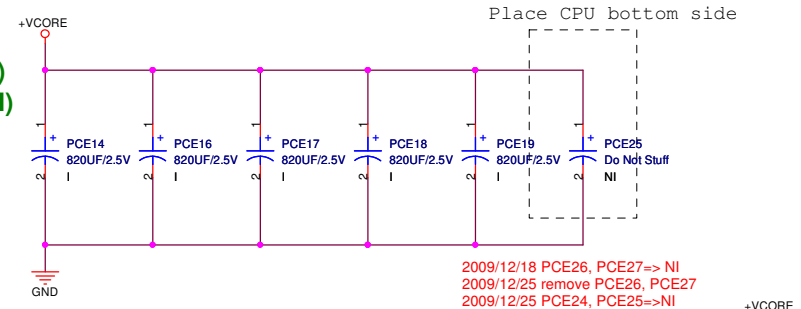


Output CAP

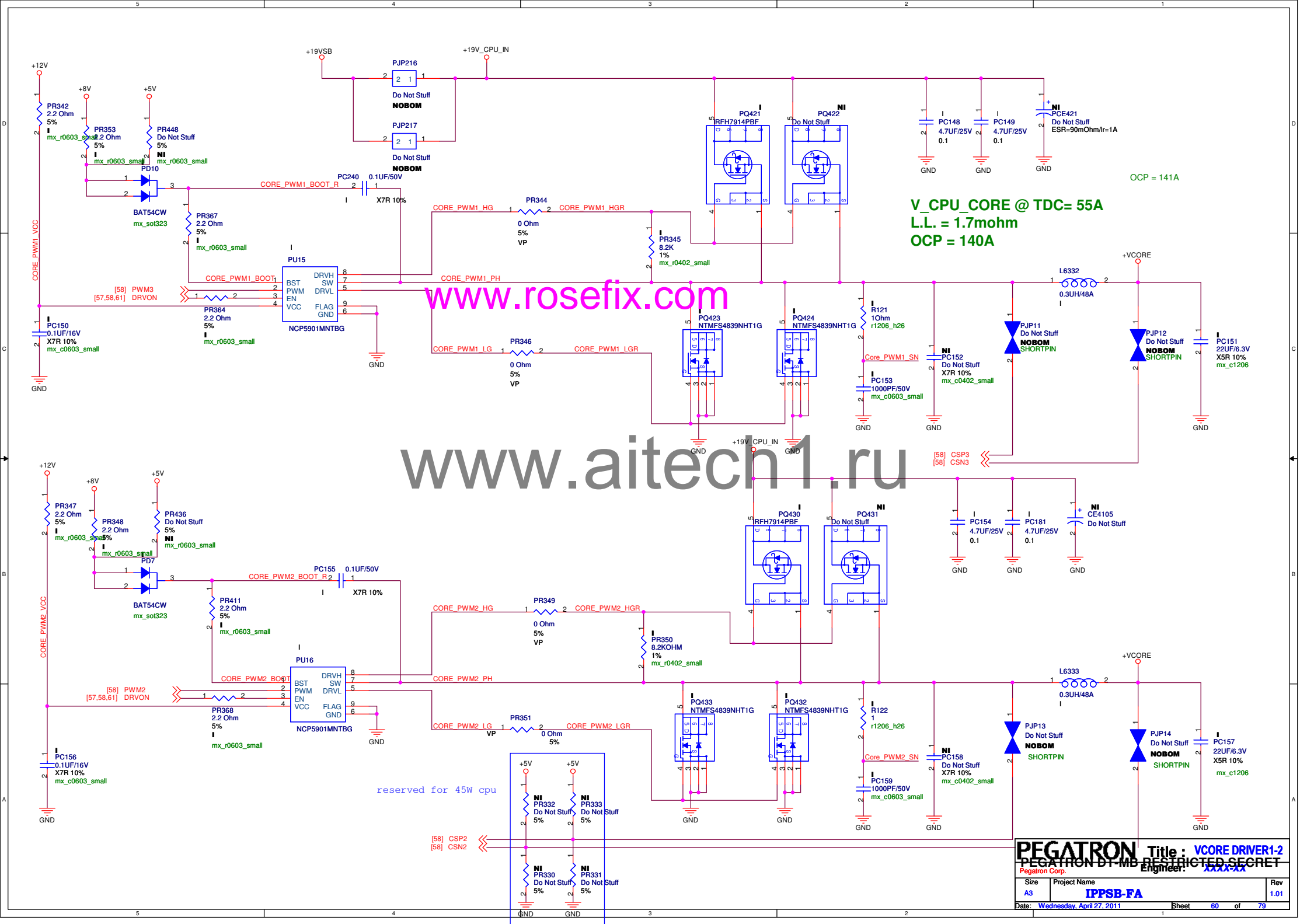
Table 30-2. Decoupling Requirements

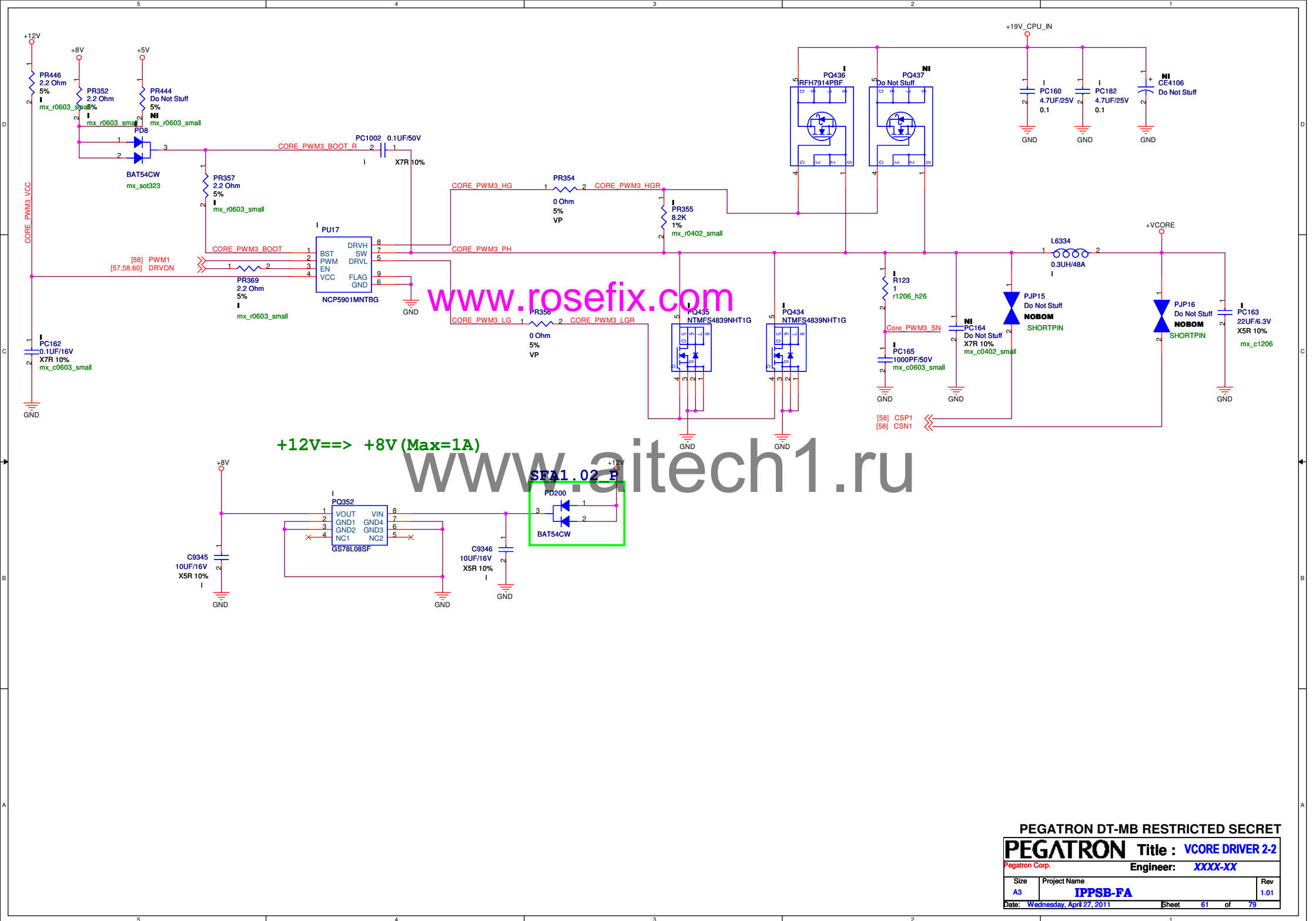
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCORE DRIVER 2-2

Pegatron Corp. Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPPSB-FA	1.01
Date: Wednesday, April 27, 2011		Sheet 61 of 79

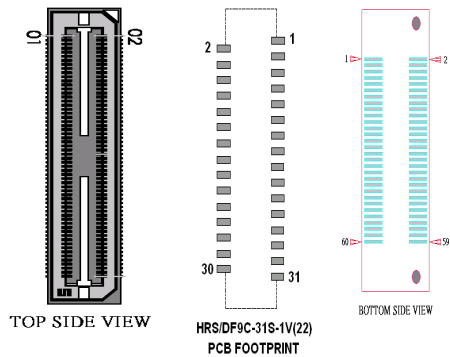
BOTTOM SIDE VIEW

**PEGATRON** Title : PCH XDP DEBUG

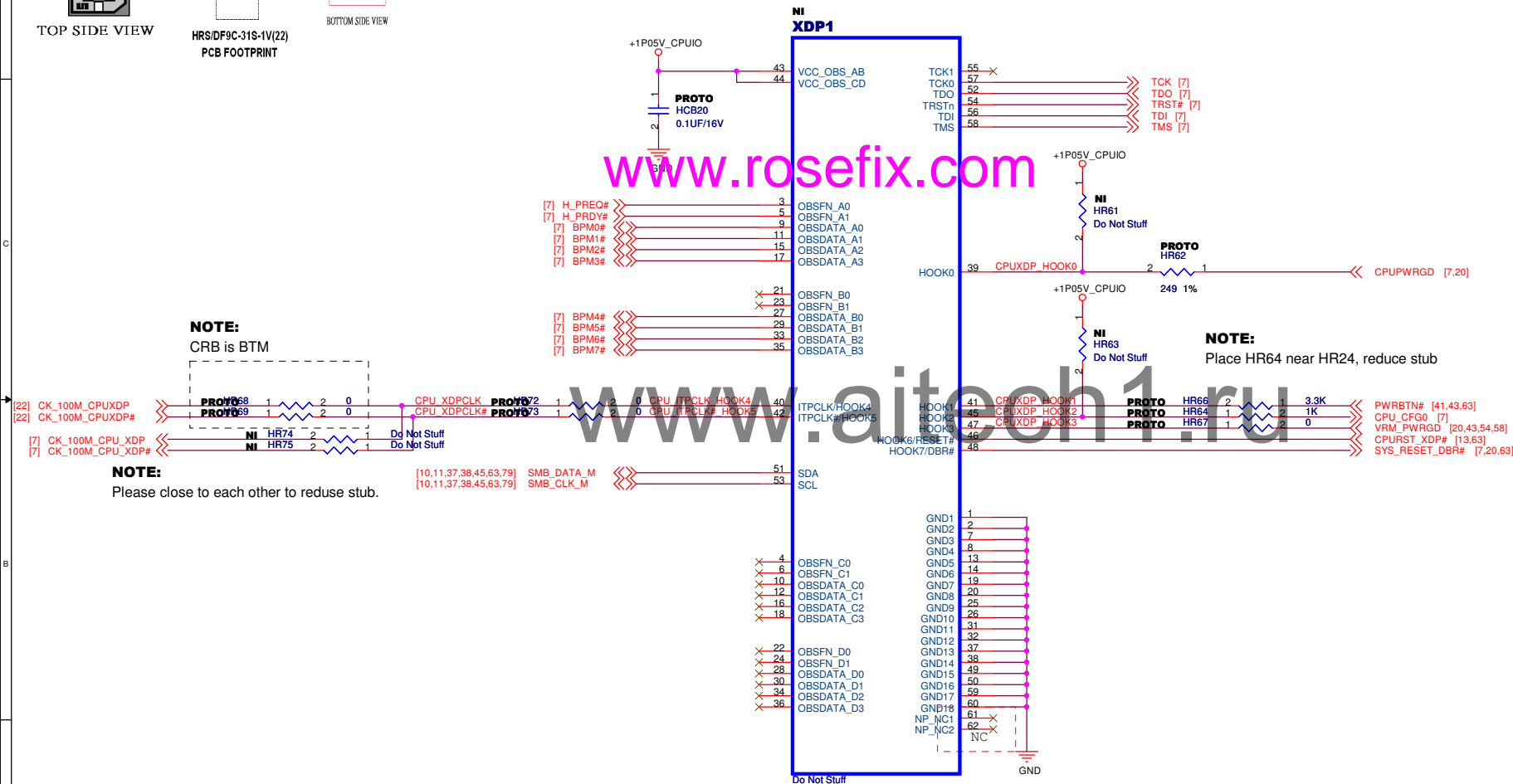
PEGATRON CORPORATION Engineer: XXXX-XX

Size A3	Project Name IPPSB-FA	Rev 1.01
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Date: Wednesday, April 27, 2011 Sheet 63 of 79



INTEL CPU XDP DEBUG PORT



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU XDP DEBUG

PEGATRON CORPORATION Engineer: XXXX-XX

Size	Project Name	Rev
A3	IPPSB-FA	1.01

Date: Wednesday, April 27, 2011 Sheet 64 of 79

整份新增修改

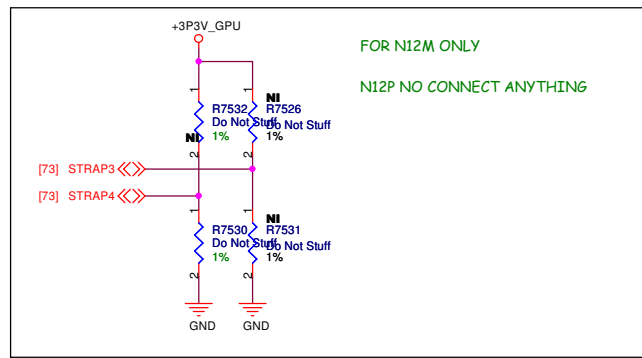
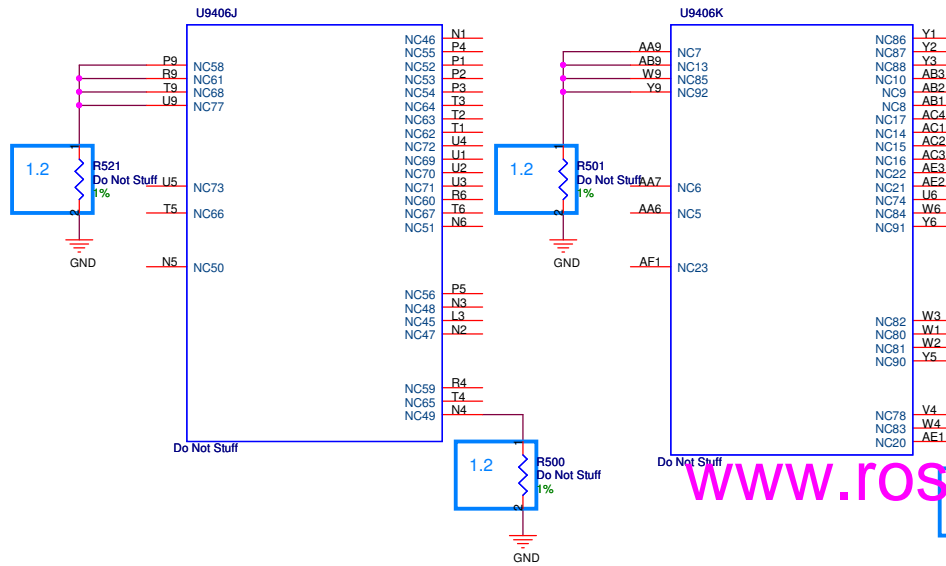
Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

NOTE:

NOTE:

Place there VGA filter components within 500 mils of the VGA connector

PEGATRON		Title : VGA CONN	
PEGATRON CORPORATION		Engineer: Jerry, Hsuan	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet	65 of 79



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ROM_SI	bit0	RAM_CFG_0	16b (64Mx16 8pcs)
	bit1	RAM_CFG_1	RAM_CFG[3:0] Definitions
	bit2	RAM_CFG_2	0x2: Hynix => H5TQ1G63BFR-12C
	bit3	RAM_CFG_3	0x3: Samsung => K4W1G1646E-HC12
			0x0010 : 15K PD

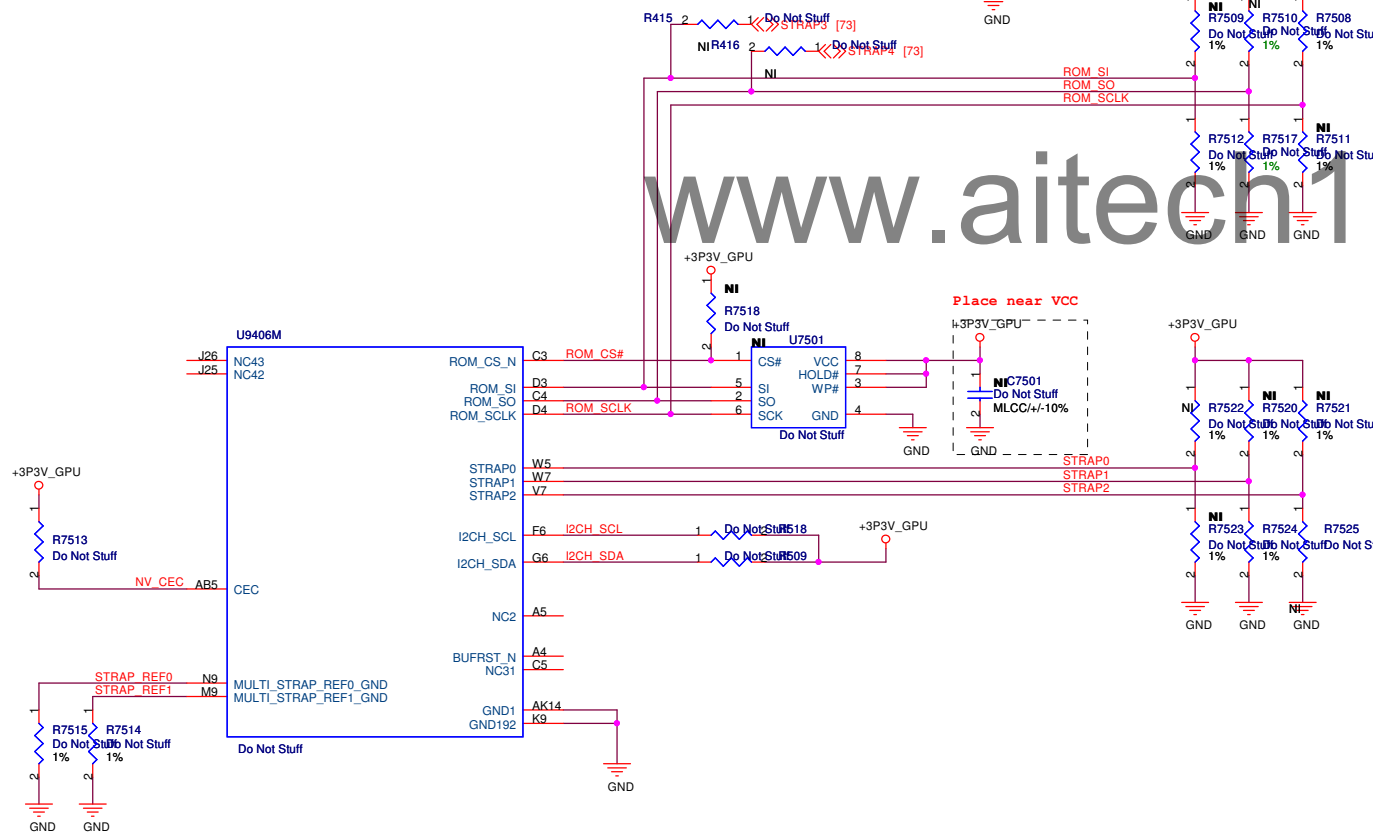
ROM_SO	bit0	VGA_DEVICE	1: VGA Device (default class code 300h)
	bit1	SMB_ALT_ADDR	0: 0x9E (default)
	bit2	FB_0_BAR_SIZE	0: 256MB (default)
	bit3	XCLK_417	0: 277M Hz (default)
			0x0001 : 10K PD
			0x0001 : 10K PD
			different

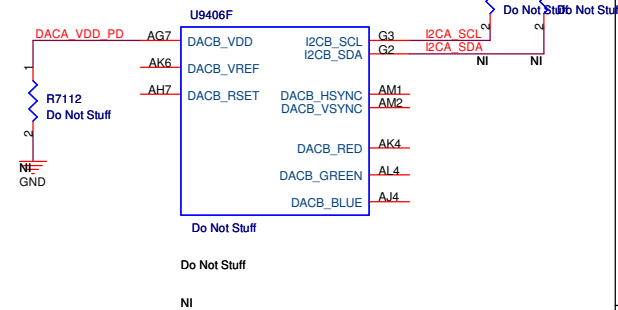
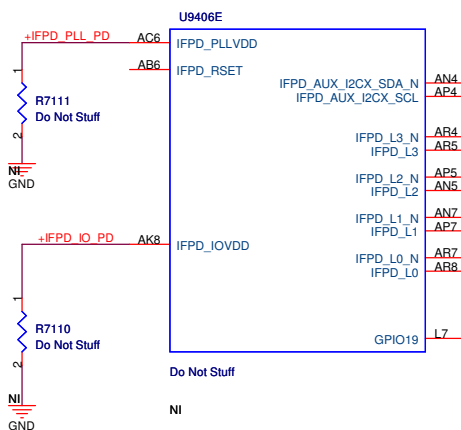
ROM_SCLK	bit0	PEX_PLL_EN_TERM	0: Disable (default)
	bit1	SLOT_CLK_CONFIG	0: GPU & MCH not share common reference clock
	bit2	SUB_VENDER	0: no vidio BIOS ROM
	bit3	PCI_DEVID_4	1: PCI_Devid[4] => 0x0DFE bit 4 = 1
			0x0011 : 35K PU
			0x0011 : 35K PU
			different

STRAP0	bit0	USER_BIT0	
	bit1	USER_BIT1	
	bit2	USER_BIT2	
	bit3	USER_BIT3	
			0x0000 : 5K PD (Panels select Default 0x0000)

STRAP1	bit0	3GIO_PADC6_LUT_ADR0	
	bit1	3GIO_PADC6_LUT_ADR1	
	bit2	3GIO_PADC6_LUT_ADR2	
	bit3	3GIO_PADC6_LUT_ADR3	
			0x6 : 35k PD (PCIE swing default)

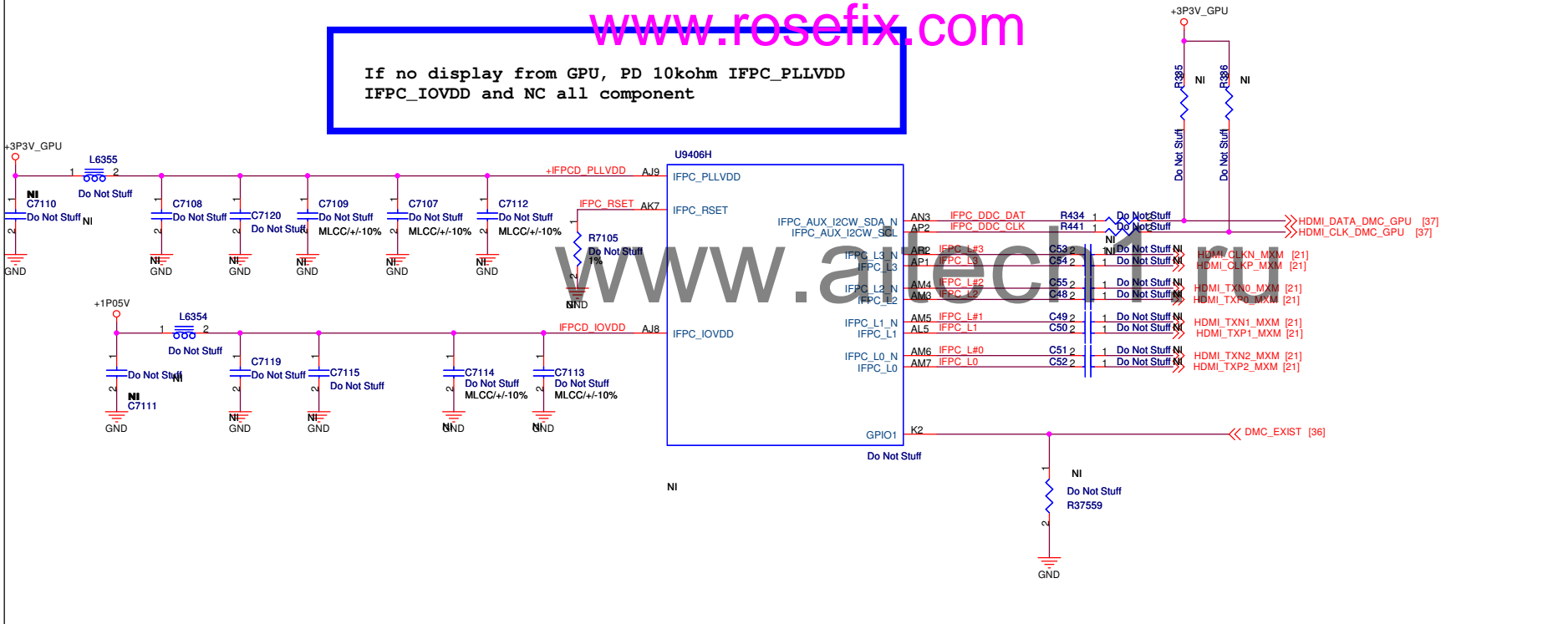
STRAP2	bit0	PCI_DEVID_0	
	bit1	PCI_DEVID_1	
	bit2	PCI_DEVID_2	
	bit3	PCI_DEVID_3	
			NI2P-6E 0x0101 : 30K PD
			NI2M-6S 0x0100 : 30K PD



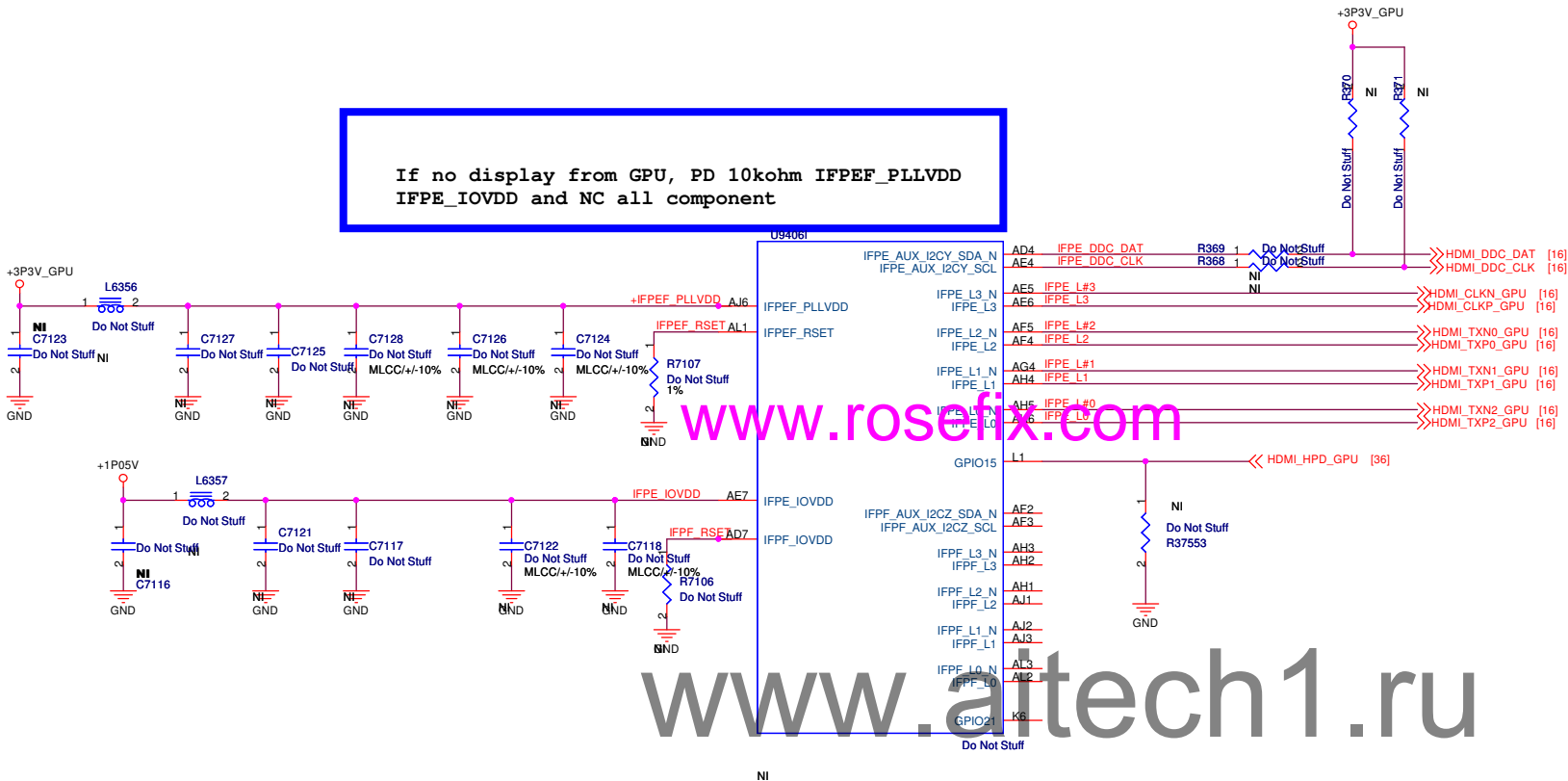


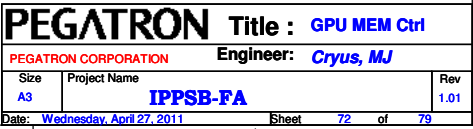
www.rosefix.com

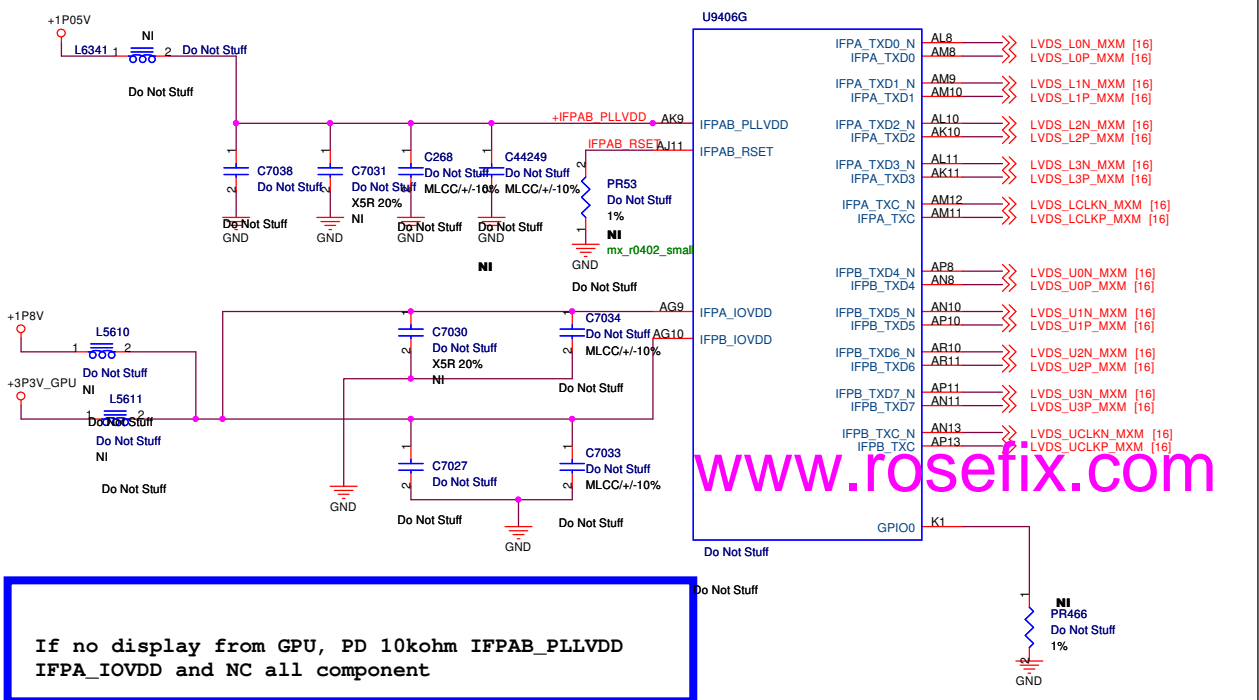
If no display from GPU, PD 10kohm IFPC_PLLVDD
IFPC_IOVDD and NC all component



If no display from GPU, PD 10kohm IFPEF_PLLVDD
IFPE_IOVDD and NC all component

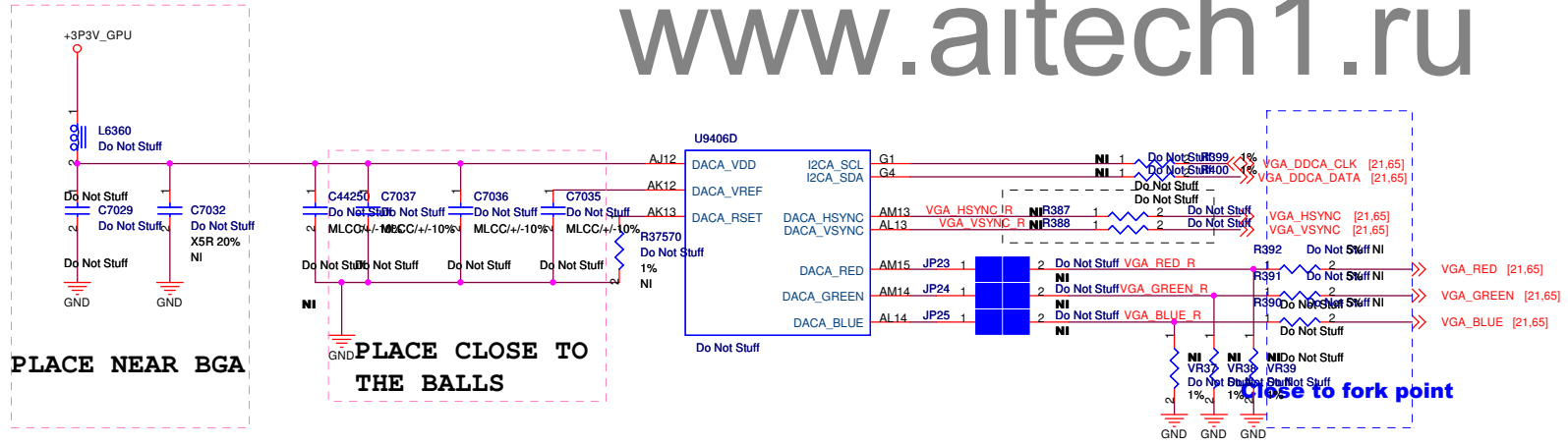




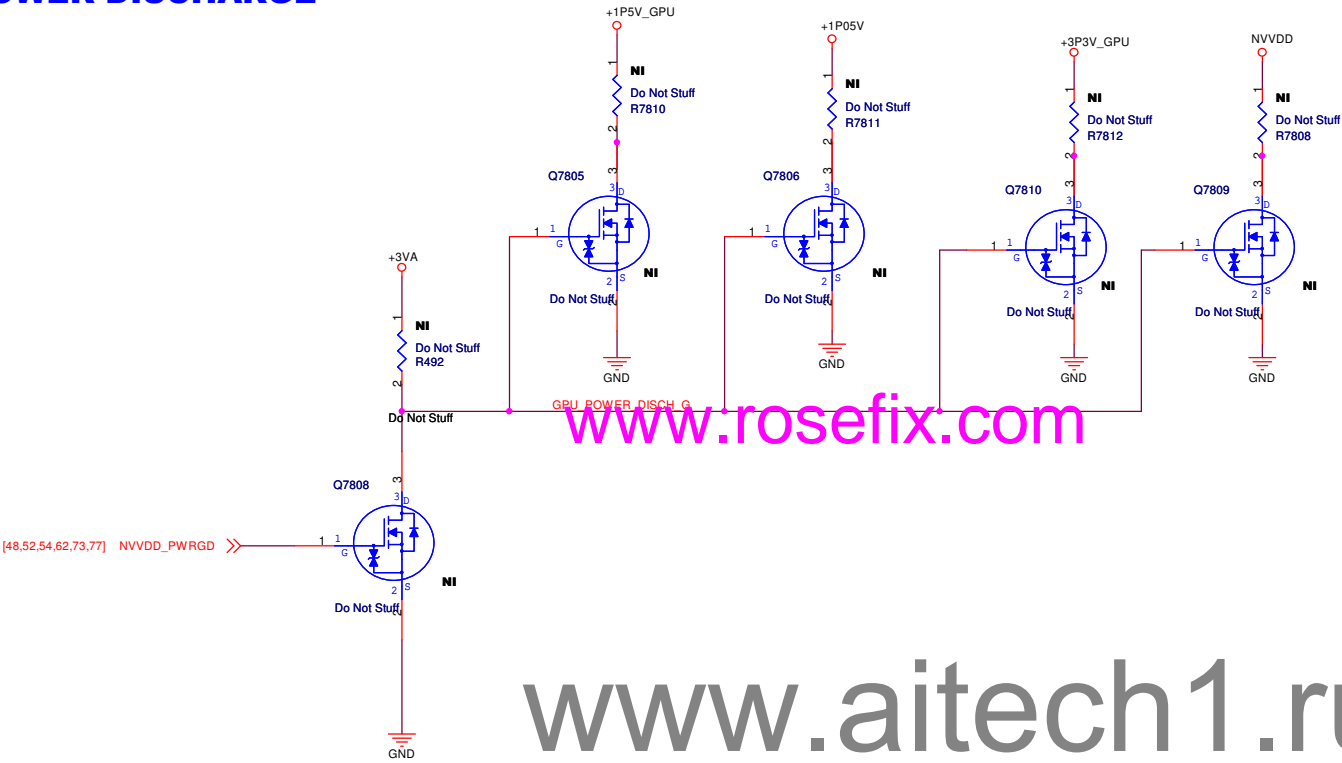


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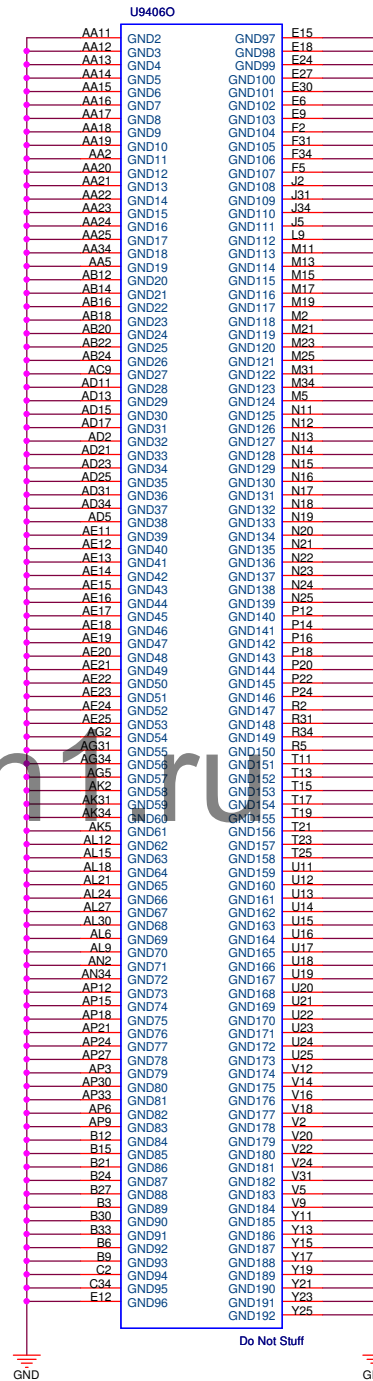
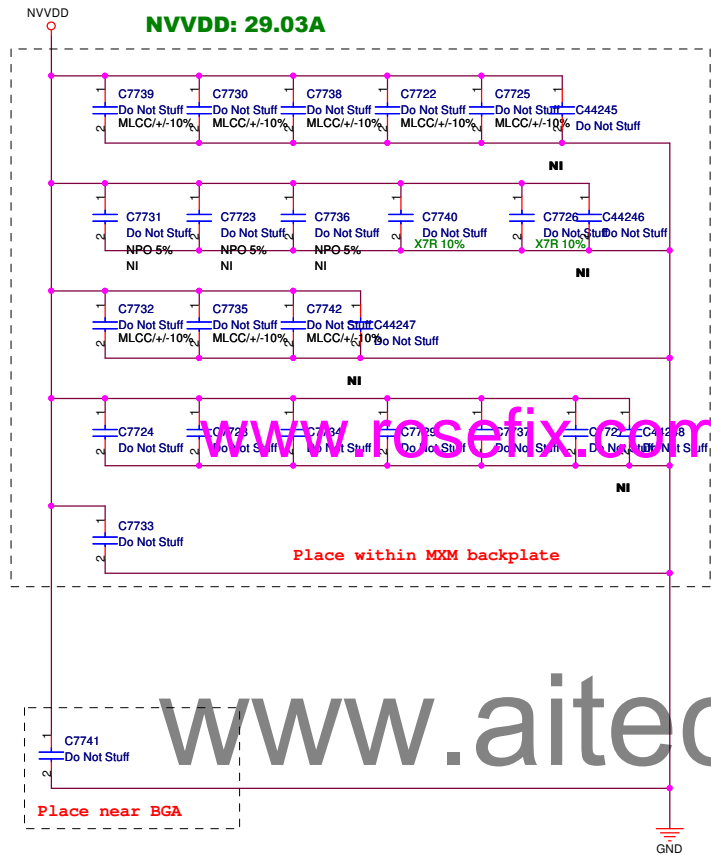
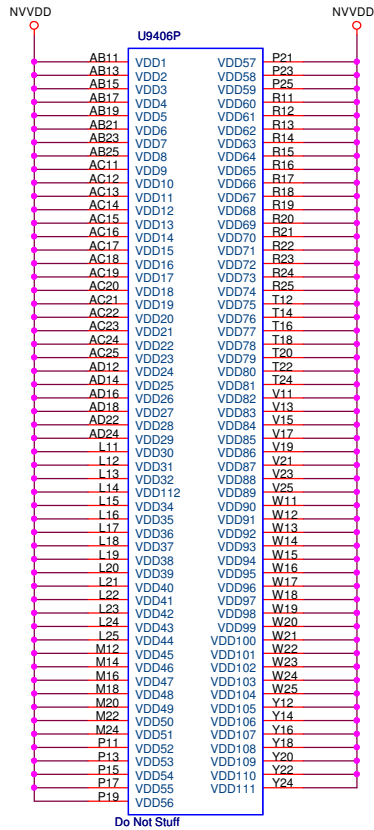


GPU POWER DISCHARGE



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12/28 新增
01/07 修改



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : GPU POWER&GND
-----------------	-----------------------

PEGATRON CORPORATION Engineer: *Cryus, MJ*

Size	Project Name	Rev
A3	UPPER BA	1.01

A3	IPPSB-FA			1.01
Date:	Tuesday, April 26, 2011	Sheet	76	of 79

19Vin.....Iin(rms)=2.28A
Trace width>100mils

PL1以此料為主09X20401C0K0
Design Rule -> NVVDD: 31.56A
TDC:22.1A
Trace width>1200mils

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BOM option

	N12M-GS	N12P-GE
PR21	50K	60.4K
PR22	294K	75K

N12M-GS

GPIO5	GPIO6	
PWRCNTL_0	PWRCNTL_1	NVVDD
L	L	0.85V
L	H	0.875V
H	L	1.00V
H	H	1.025V

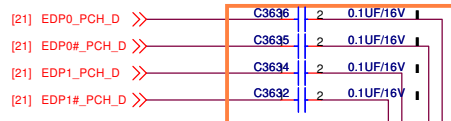
N12P-GE

GPIO5	GPIO6	
PWRCNTL_0	PWRCNTL_1	NVVDD
L	L	0.85V
L	H	0.95V
H	L	0.975V
H	H	

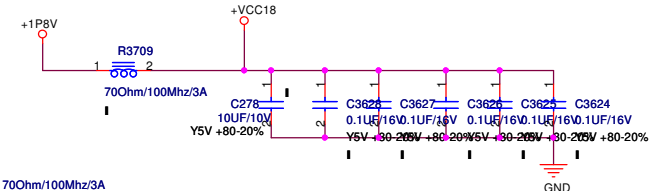
PEGATRON Title : NVVDD

PEGATRON CORPORATION Engineer: Cryus, MJ

Size A3 Project Name IPPSB-FA Rev 1.01
Date: Wednesday, April 27, 2011 Sheet 77 of 79



SFA1.04



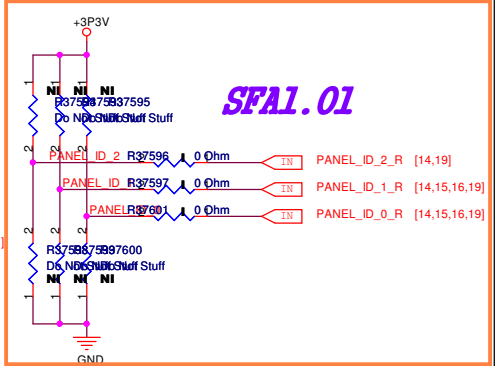
SFA1.01



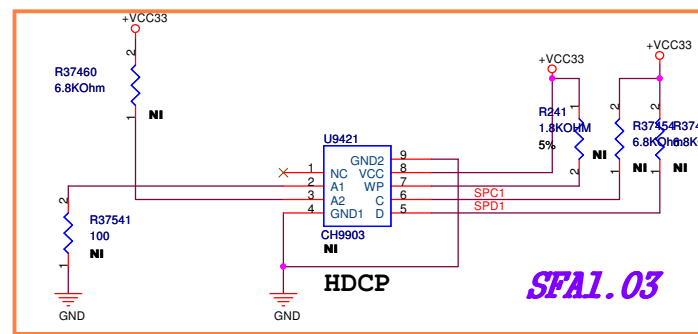
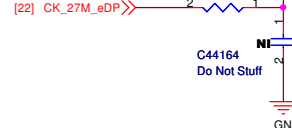
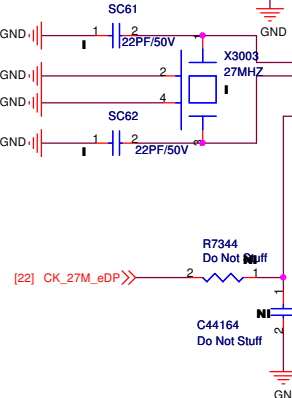
SFA1.01



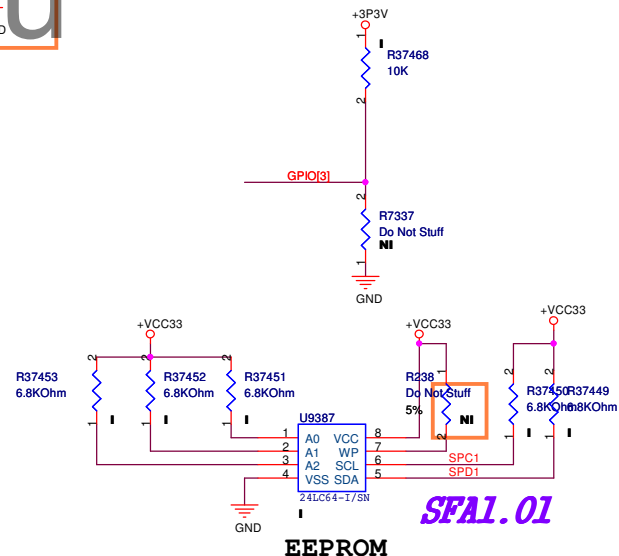
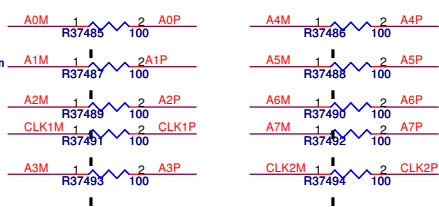
SFA1.04



SFA1.01



SFA1.03



SFA1.01

EEPROM